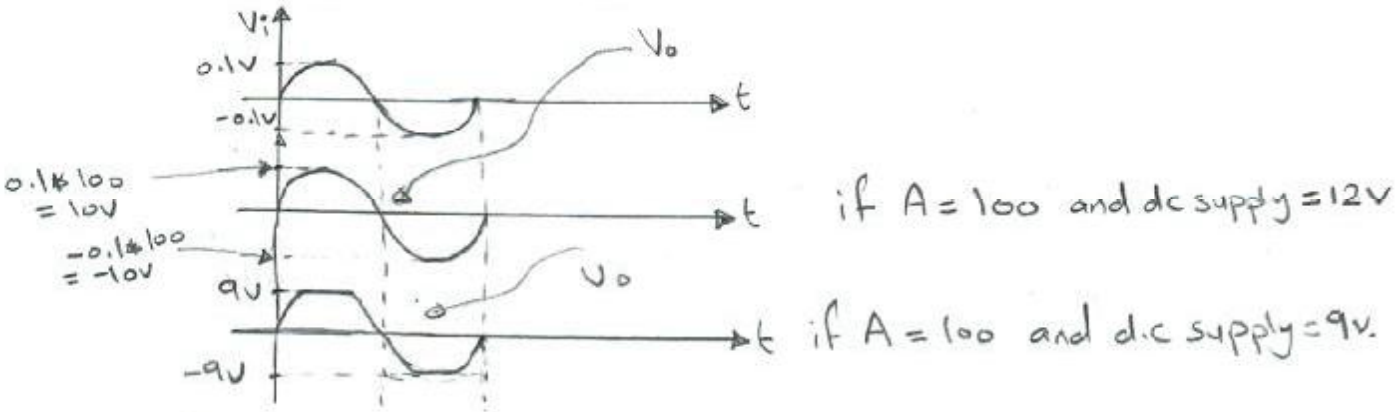
Small Signal Ac Analysis of BJTs

A transistor can be used as an amplifying device. That is, the output sinusoidal signal is greater than the input signal.

Note:

- The output of the amplifier cannot exceed the dc power level of the amplifier's dc supply. If it exceeds the dc level of the supply it will result in the clipping of the output signal.



- The analysis or design of any electronic amplifier has two components:
  1. The **dc response** of the system.
  2. The **ac response** of the system.

  Due to superposition theorem the dc response can be totally separated from the ac response and the total response of the system will be:

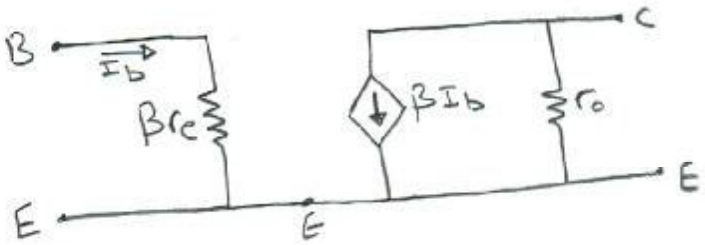
  The total response = the dc response + the ac response

  All the dc signals in an electronic amplifier will be given a notation with capital letters, as for the ac signals they are given small letters subscripts. For example (dc signals) I_B, I_C, V_{BE} and (ac signals) I_b, I_c, V_{be}.

To know the ac analysis of a transistor, an ac model for the transistor is required. Many ac models of the transistor exist in this study the r_e - model is employed.

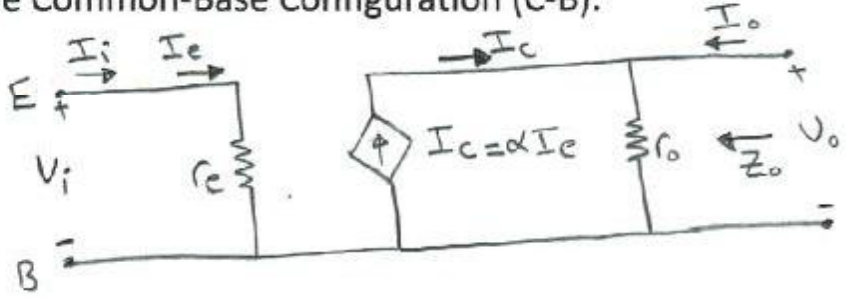
The r_e transistor model:

The Common-Emitter Configuration (C-E):



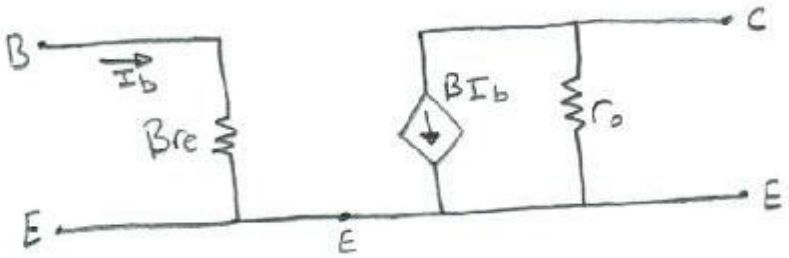
$$r_e = \frac{26mV}{I_{EQ}}$$

The Common-Base Configuration (C-B):



The Common-Collector Configuration (C-C):

For the C-C configuration the r_e -model defined for the C-E configuration is normally applied.



Note:

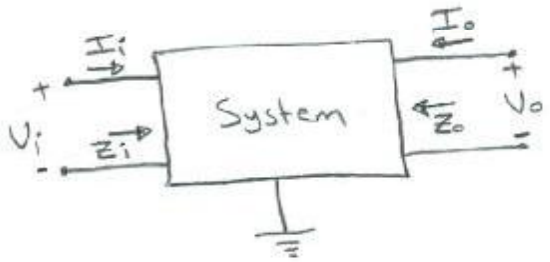
For all of the transistor configurations the ac equivalent is obtained by:

1. Setting all dc sources to zero and replacing them by a short-circuit equivalent.
2. Replacing all capacitors by a short-circuit equivalent.
3. Removing all elements bypassed by a capacitor.
4. Replacing the transistor by its ac equivalent model (r_e –model).
5. Finding the important parameters of any system (Z_i , Z_o ,A_v)

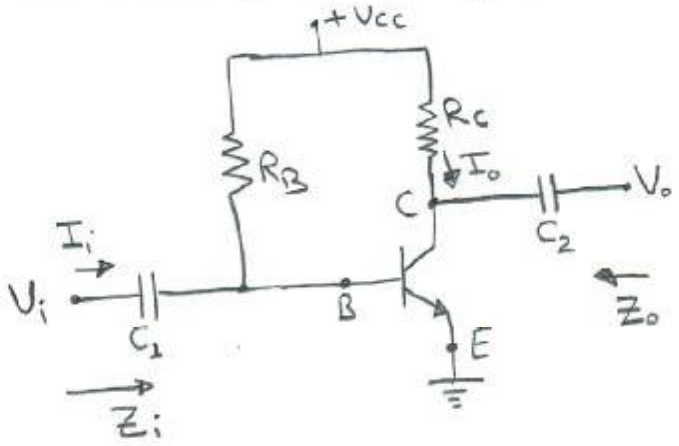
$$Z_i = \frac{V_i}{I_i}$$

$$Z_o = \frac{V_o}{I_o}$$

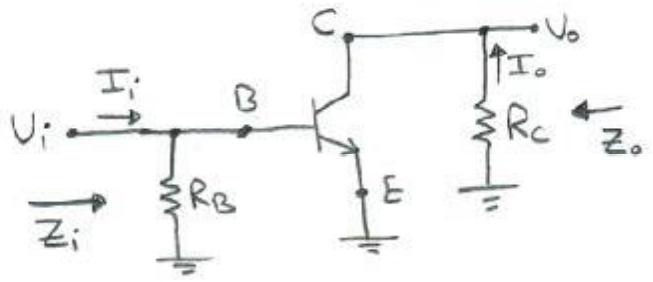
$$A_v = \frac{V_0}{V_i}$$



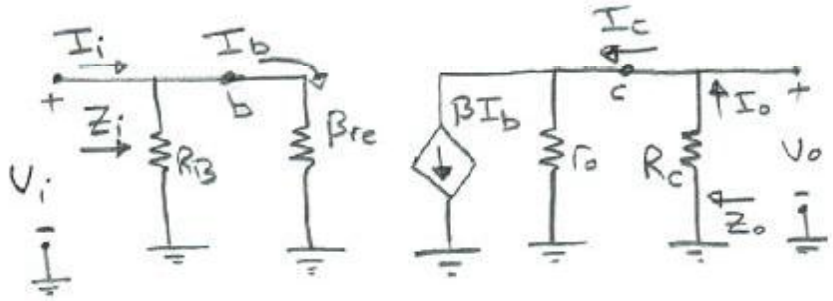
C-E Fixed-Bias Configuration Ac analysis:



Replacing all dc sources and capacitors by short circuits we get:



Replacing the transistor by its ac equivalent model (r_e –model) results in the following network:



The values of r_o and β are given in the specification sheet of the transistor. While r_e must be determined from the dc analysis:

$$r_e = \frac{26mV}{I_{EQ}}$$

To find Z_i :

$$Z_i = \frac{V_i}{I_i} = R_B//\beta r_e$$

$$\boxed{Z_i = R_B//\beta r_e}$$

$Z_i \cong \beta r_e$ if $R_B \geq 10\beta r_e$

Z_o

The output resistance is obtained by setting the source voltage (V_s) to zero and the load resistance R_L to infinity and by driving the output terminals from a generator V_2. If the current drawn from V_2 is I_2 then:

$$Z_o = \frac{V_2}{I_2}$$

If $V_s = 0$, $V_i = 0$ and $I_i = I_b = 0$ resulting in $\beta I_b = 0$ and

$Z_o = R_C // r_o$

$Z_o \cong R_C$ if $r_o \geq 10R_C$

A_v

$$V_o = -\beta I_b (R_C // r_o)$$

$$I_b = \frac{V_i}{\beta r_e}$$

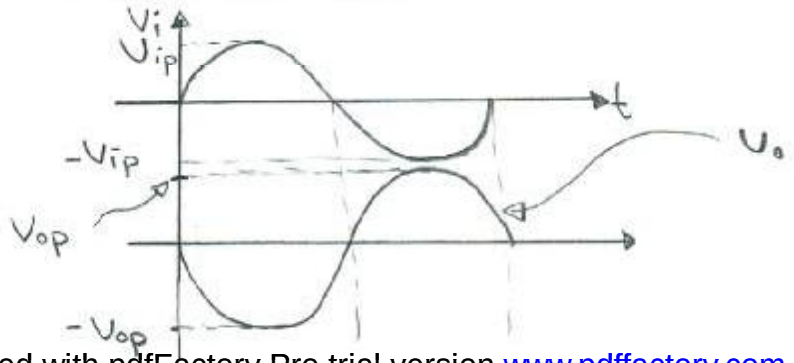
$$V_o = -\beta\left(\frac{V_i}{\beta r_e}\right)(R_C // r_o)$$

$$A_v = \frac{V_o}{V_i} = -\frac{(R_C // r_o)}{r_e}$$

$$A_v = -\frac{R_C}{r_e}$$ if $r_o \geq 10R_C$

Note:

The negative sign in the A_v equation shows that a 180° phase shift exists between the input and the output.

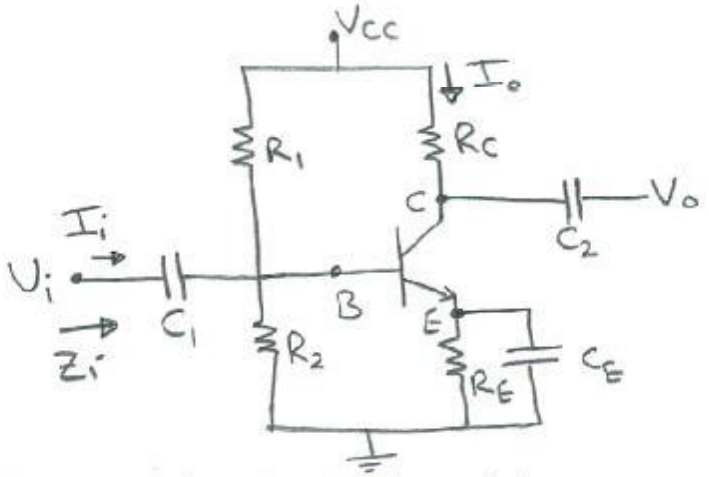


Vip:- the peak of the input waveform

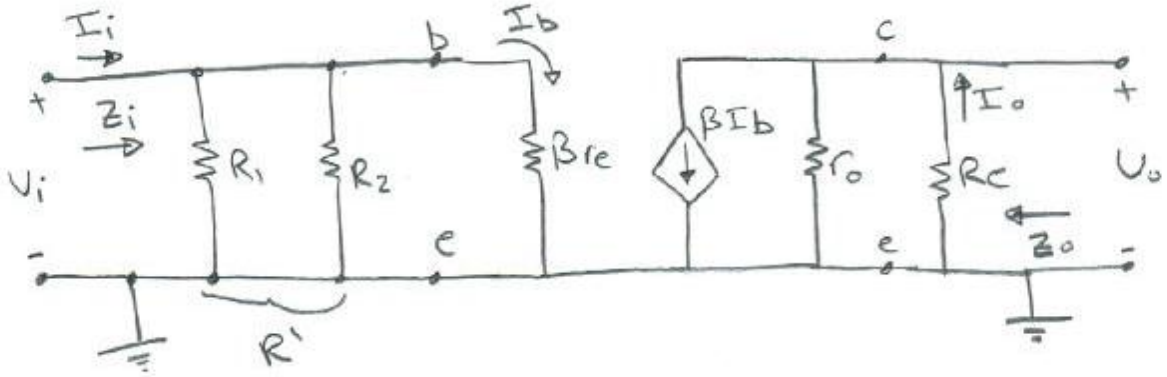
Vop:- the peak of the o/p waveform

Example 5.1

Voltage Divider Bias Configuration Ac Analysis:



Its ac equivalent circuit is shown below:



Z_i

$$Z_i = R_1 \parallel R_2 \parallel \beta r_e$$

Z_o

$$Z_o = R_c \parallel r_o$$

$$Z_o \cong R_c \quad \text{if } r_o \geq 10 R_c$$

A_v

$$V_o = -(\beta I_b)(R_c \| r_o)$$

$$I_b = \frac{V_i}{\beta r_e}, \quad V_o = -\beta\left(\frac{V_i}{\beta r_e}\right)(R_c \| r_o)$$

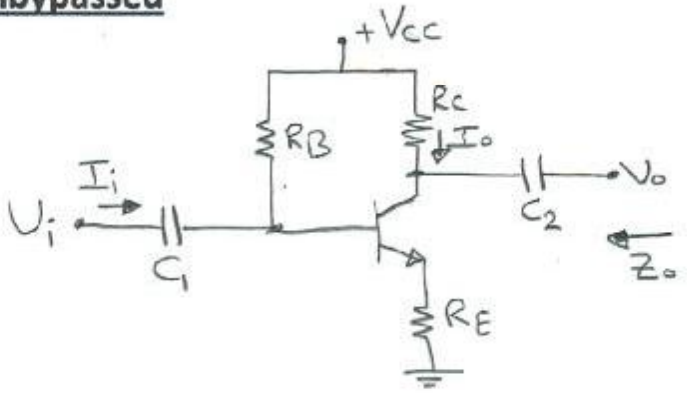
$$A_v = \frac{V_o}{V_i} = \frac{-R_c \| r_o}{r_e} \qquad A_v \cong -\frac{R_c}{r_e} \text{ if } r_o \geq 10 R_c$$

Note: the negative sign shows a 180° phase shift between V_o and V_i.

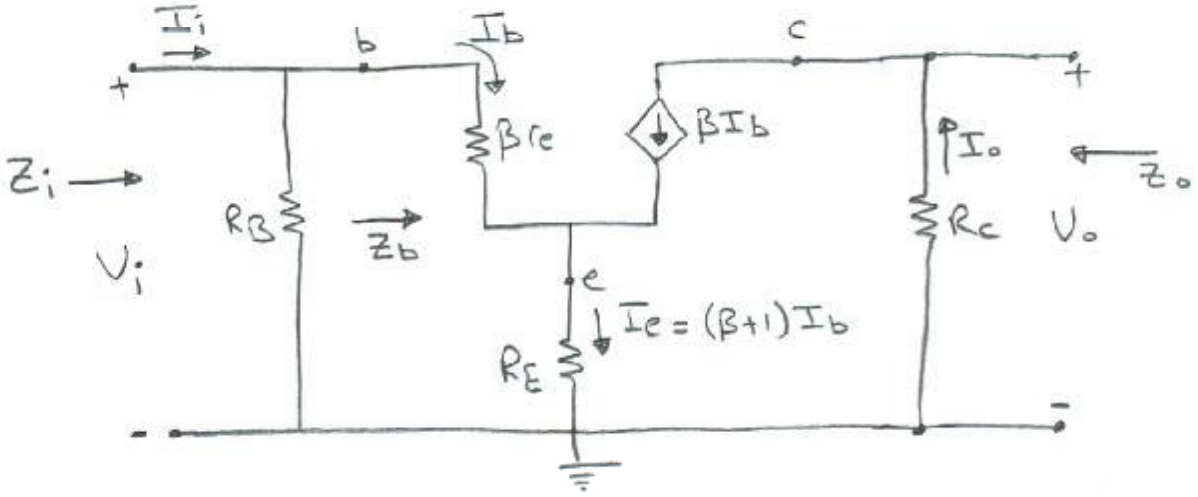
Example 5.2

C-E Emitter-Bias Configuration:

Unbypassed



The ac equivalent circuit is shown in the following figure:



In the ac equivalent circuit r_o is absent. The presence of r_o complicates the analysis very much and considering the fact that in most situations its effect can be ignored.

First applying Kirchhoff's voltage law to the input side of the ac equivalent circuit results in:

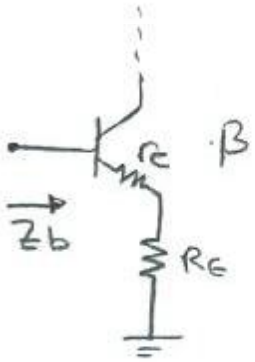
$$V_i = I_b \beta r_e + I_e R_E$$

$$V_i = I_b \beta r_e + (\beta+1) I_b R_E$$

$$Z_b = \frac{V_i}{I_b} = \beta r_e + (\beta+1) R_E$$

The result as displayed in the figure below reveals that the input impedance of a transistor with an unbypassed resistor R_E is determined by

$$\boxed{Z_b = \beta r_e + (\beta+1) R_E}$$



Because $\beta \gg 1$ then $Z_b \cong \beta r_e + \beta R_E$

$$\boxed{Z_b = \beta (r_e + R_E)}$$

because $R_E \gg r_e$ then $\boxed{Z_b \cong \beta R_E}$

Z_i

$$\boxed{Z_i = R_B \| Z_b}$$

Z_o

$$Z_o = R_C$$

A_v

$$I_b = \frac{V_i}{Z_b}$$

$$V_o = -I_o R_C = -\beta I_b R_C$$

$$= -\beta \left(\frac{V_i}{Z_b}\right) R_C$$

$$A_V = \frac{V_o}{V_i} = -\frac{\beta R_C}{Z_b}$$

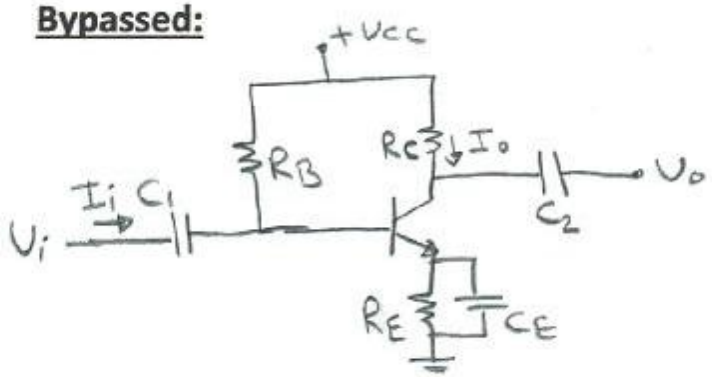
$$Z_b \cong \beta(r_e + R_E)$$

$$A_V = \frac{V_o}{V_i} \cong -\frac{R_C}{r_e + R_E}$$

and for the approximation $Z_b \cong \beta R_E \Rightarrow A_V \cong -\frac{R_C}{R_E}$

Note: also the negative sign reveals a phase shift between V_o and V_i.

Bypassed:



If R_E is bypassed than the same ac equivalent of the fixed-bias configuration is obtained and the same equations for Z_i, Z_o, and A_v are applied.

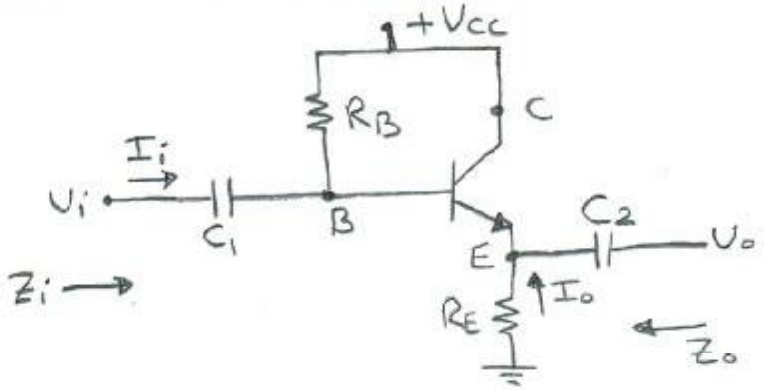
Example 5.3

Example 5.4

Example 5.5

Example 5.6

Emitter-Follower Configuration:

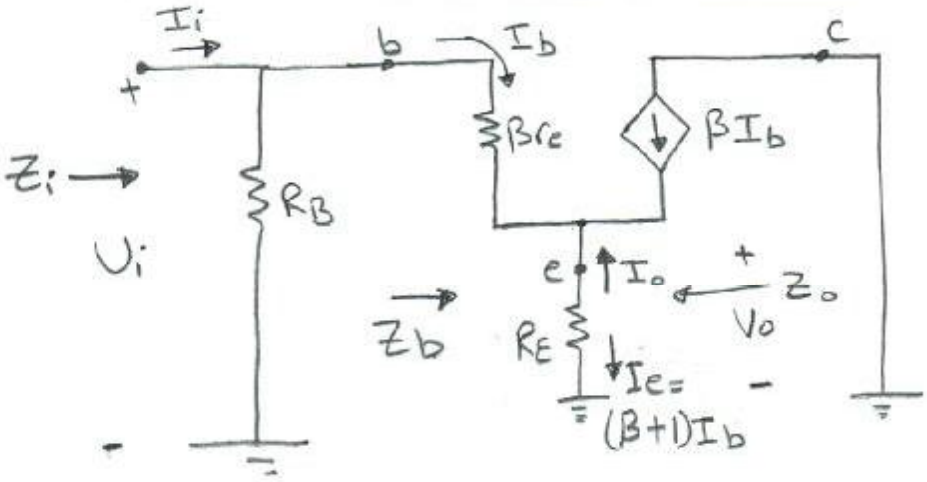


The terminology "emitter-follower" is given to this configuration because the output V_o from the emitter follows the magnitude of the input voltage V_i and in phase with V_i.

$A_v \cong 1$ for the emitter-follower configuration.

Note: the emitter-follower is used as a buffer between stages because the emitter follower provides high input impedance and low output impedance and its voltage gain is approximately equal to 1.

The ac equivalent circuit for the emitter-follower shown above is as in the following figure: (r_o is absent to simplify the calculations $r_o \geq 10R_E$)



Z_i $\boxed{Z_i = R_B \| Z_b}$

$\boxed{Z_b = \beta r_e + (\beta+1) R_E}$

$\boxed{Z_b \cong \beta (r_e + R_E)}$

$\boxed{Z_b \cong \beta R_E}$ $R_E \gg r_e$

Z_o

$I_b = \frac{V_i}{Z_b}$

$I_e = (\beta+1) I_b = (\beta+1) \frac{V_i}{Z_b}$

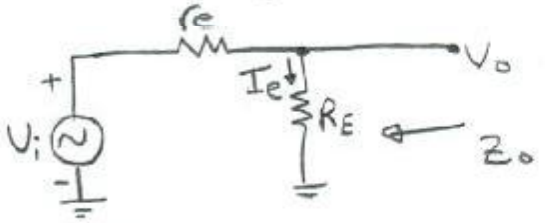
Substitute the equation for Z_b we get:-

$$I_e = \frac{(\beta+1) V_i}{\beta r_e + (\beta+1) R_E}$$

$$I_e = \frac{V_i}{[\beta r_e / (\beta+1)] + R_E}$$

$(\beta+1) \cong \beta$ $\therefore \frac{\beta r_e}{\beta+1} \cong \frac{\beta r_e}{\beta} = r_e$

$\boxed{I_e \cong \frac{V_i}{r_e + R_E}}$ from this equation the following network is constructed :-



From this network Z_o is determined by setting $V_i = 0$ we get:- $\boxed{Z_o = R_E \| r_e}$ and $\boxed{Z_o \cong r_e}$ since $R_E \gg r_e$

A_V

$V_o = \frac{R_E V_i}{R_E + r_e}$ from the network constructed above.

$$\boxed{A_V = \frac{V_o}{V_i} = \frac{R_E}{R_E + r_e}}$$

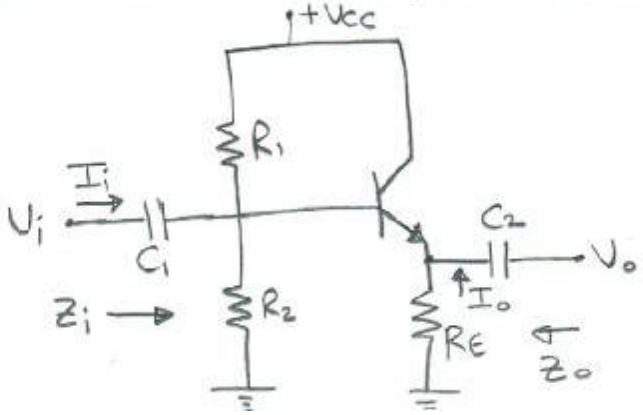
because $R_E \gg r_e$ then $r_e + R_E \cong R_E$ $\therefore \boxed{A_V \cong 1}$

Note: V_o and V_i are in phase.

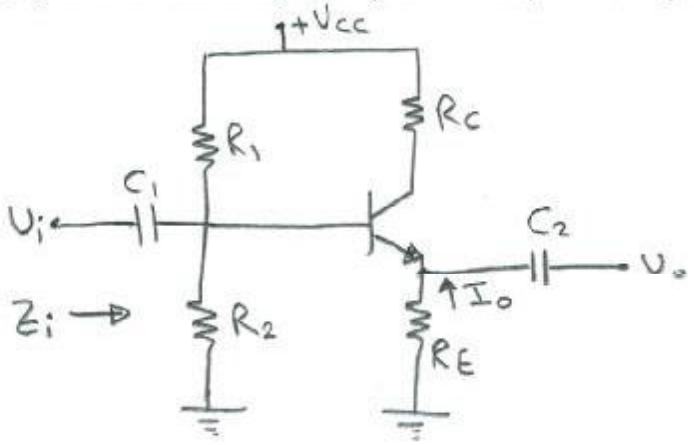
Example 5.7

Other emitter-follower configurations are shown below:

For the first network (shown below) all equations are the same as the previous emitter-follower the only change is that R_B is replaced by $R`=R_1\backslash\backslash R_2$.



For the second network also all equations are the same and only R_B is replaced by $R_1\backslash\backslash R_2$. The effect of R_C is only on the Q-point of operation.

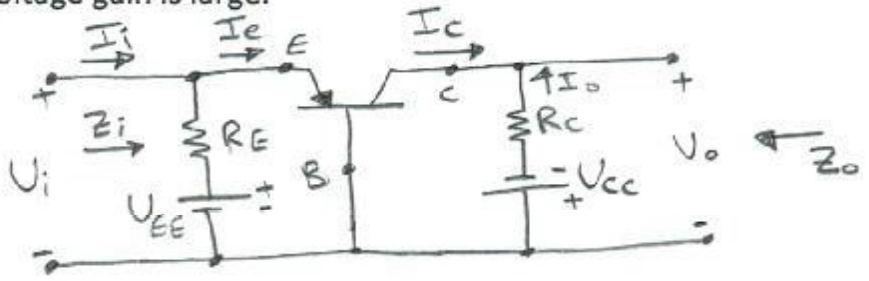


Common-Base Configuration:

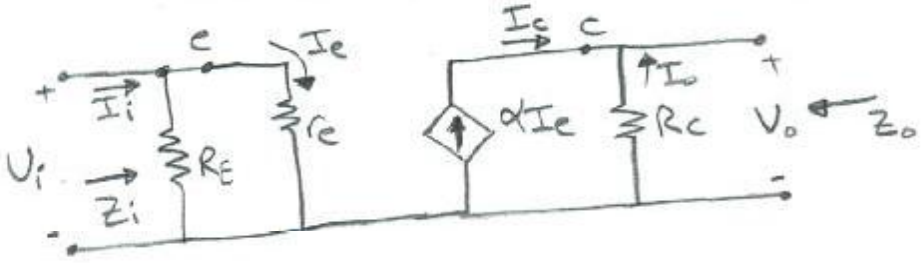
The common-base amplifier has:

1. Low input impedance.
2. High output impedance.

3. Current gain less than 1.
4. Voltage gain is large.



The ac equivalent circuit of the C-B configuration is shown below:



Note: r_o is not included in the ac equivalent because its value is in the megaohms range and can be ignored in parallel with the resistor R_C.

Z_i

$$Z_i = R_E \| r_e$$

Z_o

$$Z_o = R_C$$

A_v

$$V_o = -I_o R_C = -(-I_C) R_C = \alpha I_e R_C$$

$$I_e = \frac{V_i}{r_e}$$

$$V_o = \alpha \left(\frac{V_i}{r_e}\right) R_C$$

$$A_V = \frac{V_o}{V_i} = \frac{\alpha R_C}{r_e} \cong \frac{R_C}{r_e}$$

A_i Assuming that $R_E \gg r_e$ yields :-

$$I_e = I_i$$

$$I_o = -\alpha I_e = -\alpha I_i$$

$$A_i = \frac{I_o}{I_i} = -\alpha \cong -1$$

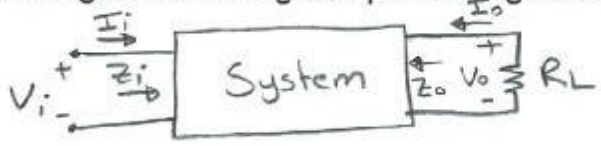
Note: A_V has a positive sign, this means that V_o and V_i are in phase.

Example 5.8

The Current Gain: (A_i)

For all the previous configurations only the voltage gain was derived due to its importance. For each transistor configuration, the current gain can be determined directly from the voltage gain, the defined load, and the input impedance.

The derivation of the equation for finding the current gain (A_i) as a function of A_v can be found using the following two-port configuration:



$$A_i = \frac{I_o}{I_i}$$

$$I_i = \frac{V_i}{Z_i} \quad \text{and} \quad I_o = -\frac{V_o}{R_L}$$

$$\therefore A_i = \frac{I_o}{I_i} = \frac{\frac{-V_o}{R_L}}{\frac{V_i}{Z_i}} = -\frac{V_o}{V_i} * \frac{Z_i}{R_L}$$

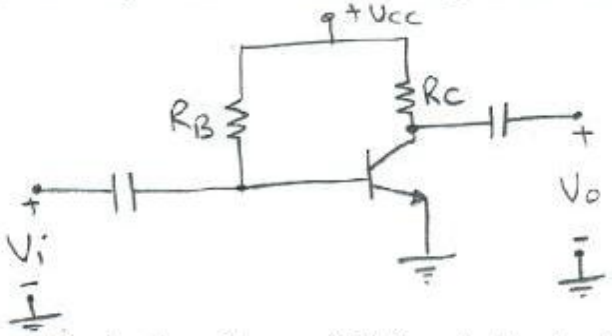
$$\boxed{A_{iL} = -A_{VL} * \frac{Z_i}{R_L}}$$

Note: the value of R_L is defined by the location of V_o and I_o.

Effect of R_L and R_S:

Z_i, Z_o, and A_v found in the previous sections are for an unloaded amplifier and with the input voltage directly connected to a terminal of the transistor. If a load resistance (R_L) is added to the output terminal and a source with an internal resistance (R_S) is used then the equations for Z_i, Z_o, and A_v will change.

Take for example the fixed-bias configuration shown in the following figure:



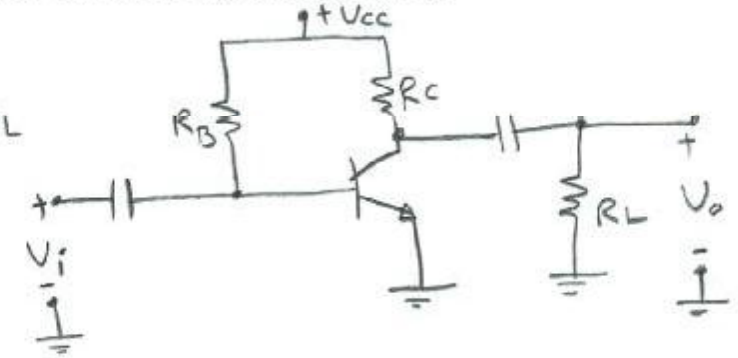
$$A_{V_{NL}} = \frac{V_o}{V_i}$$

Because the load resistance (R_L) is not attached the voltage gain is reffered to as the no-load gain and given by:

$$A_{V_{NL}} = \frac{V_o}{V_i}$$

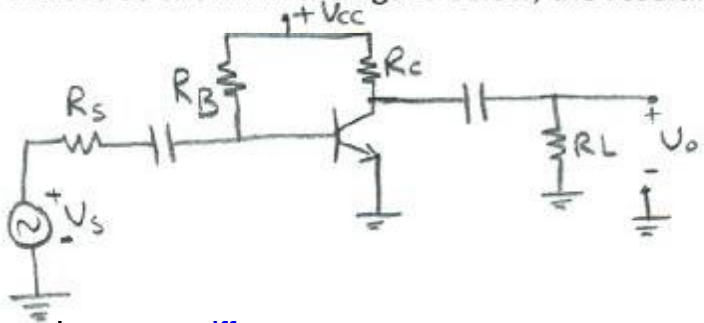
While if a load R_L is connected to the output as shown in the figure below, it will change the overall gain of the system. The loaded gain is given by:

$$A_{V_L} = \frac{V_o}{V_i} \text{ with } R_L$$



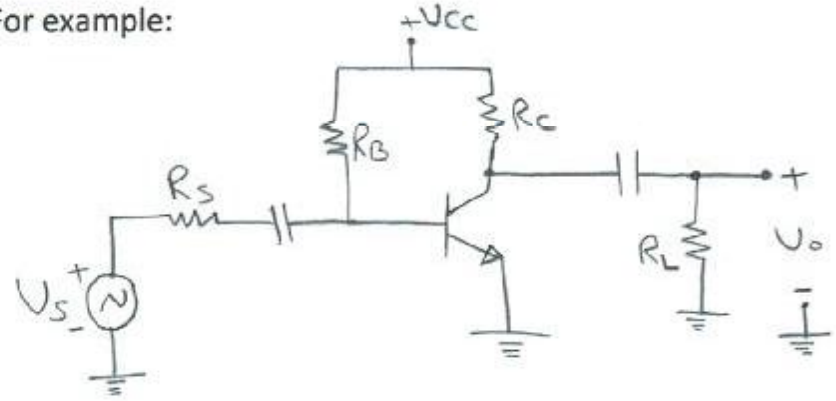
If RL and R_S are both introduced as shown in the figure below, the resulting gain is given by

$$A_{V_S} = \frac{V_o}{V_S}$$

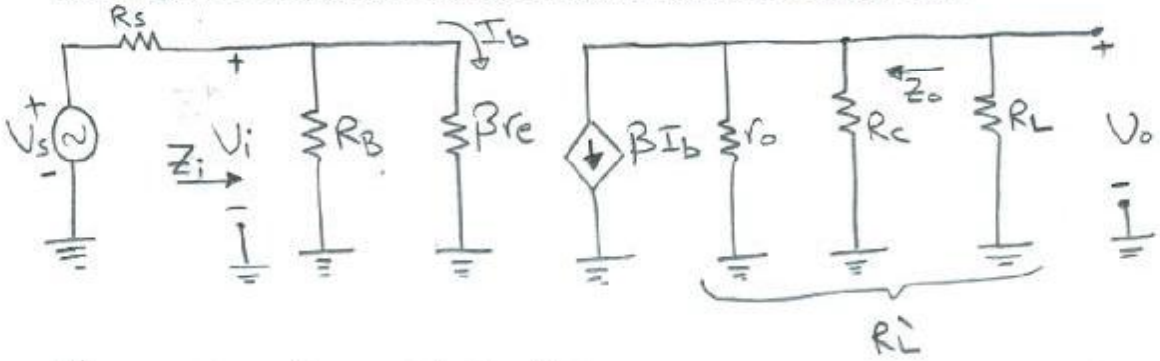


The same approach to analyze circuits with no load is employed for circuits with R_L and R_s which is to draw the ac equivalent circuit of the network and find the important parameters (Z_i, Z_o, and A_v).

For example:



Drawing the ac equivalent circuit results in the following circuit:



$$R_L' = r_o \,||\, R_c \,||\, R_L \cong R_c \,||\, R_L$$

$$V_o = -\beta I_b R_L' = -\beta I_b (R_c \,||\, R_L)$$

$$\because I_b = \frac{V_i}{\beta r_e}$$

$$\therefore V_o = -\beta \left(\frac{V_i}{\beta r_e}\right)(R_c \,||\, R_L)$$

$$\therefore \boxed{A_{VL} = \frac{V_o}{V_i} = \frac{-(R_c \,||\, R_L)}{r_e}}$$

$$Z_i = R_B \,//\, \beta r_e$$

$$Z_o = R_c \,//\, r_o$$

$$A_{VS} = \frac{V_o}{V_S} = \frac{V_o}{V_i} * \frac{V_i}{V_S}$$

$$V_i = \frac{Z_i V_S}{Z_i + R_S}$$

$$\frac{V_i}{V_S} = \frac{Z_i}{Z_i + R_S}$$

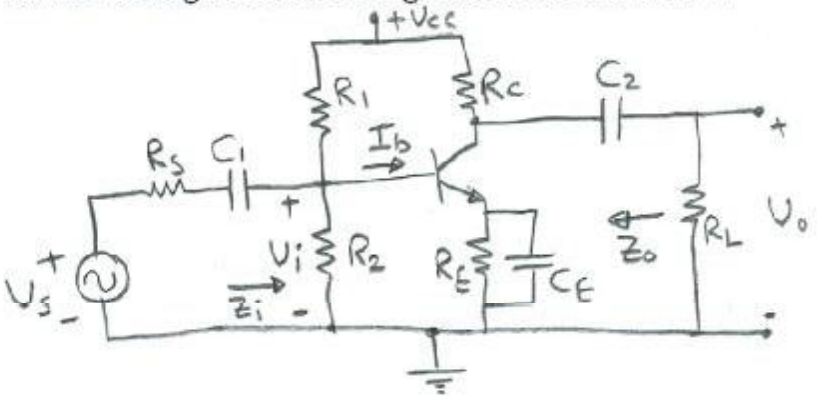
$$A_{VS} = \frac{V_o}{V_S} = A_{VL} * \frac{Z_i}{Z_i + R_S}$$

$$A_{VS} = \frac{Z_i}{Z_i + R_S} A_{VL}$$ since $\frac{Z_i}{Z_i + R_S} < 1$

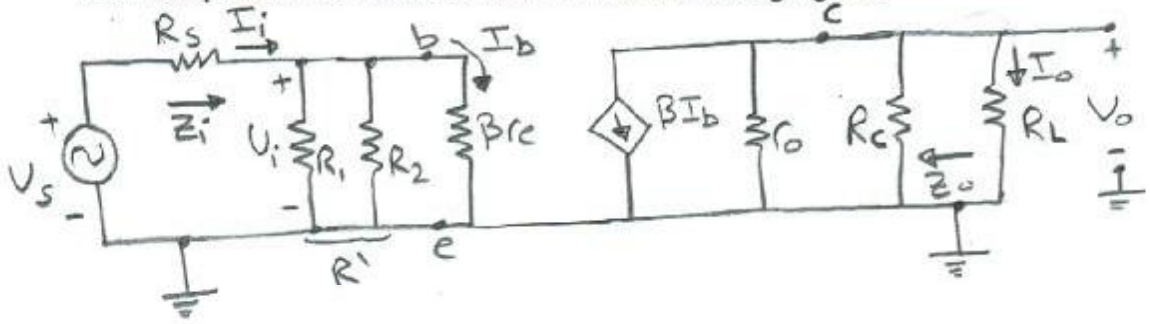
$\therefore A_{VS} < A_{VL}$

Example 5.11

For the voltage divider configuration shown below:



The ac equivalent circuit is shown in the following figure:



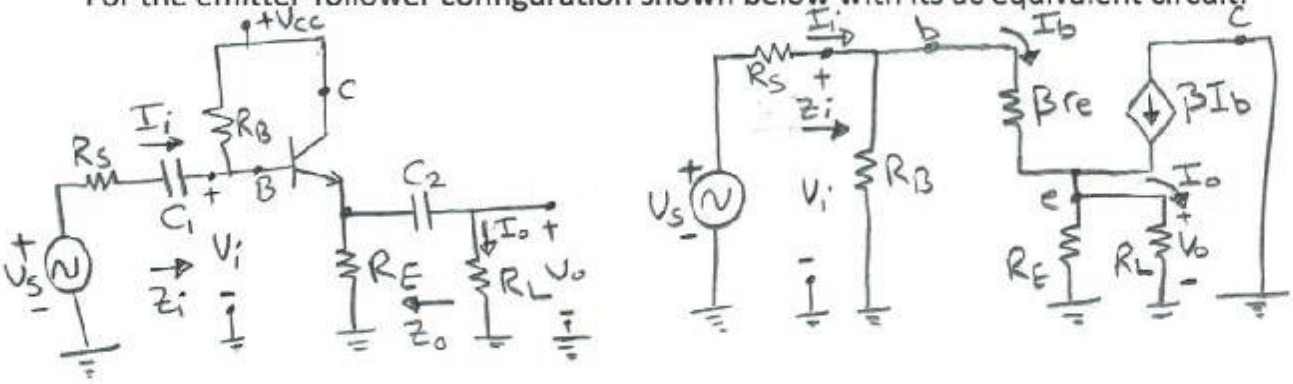
$$A_{VL} = \frac{V_o}{V_i} = -\frac{R_c \| R_L}{r_e}$$

$$Z_i = R_1 \| R_2 \| \beta r_e$$

$$Z_o = R_c \| r_o$$

$$A_{VS} = \frac{Z_i}{Z_i + R_S} A_{VL}$$

For the emitter-follower configuration shown below with its ac equivalent circuit:



The only difference from the unloaded amplifier is the parallel combination of R_E and R_L and the addition of the source resistance. So the quantities of interest can be found by simply replacing each R_E by R_E // R_L. as in the following:-

$$A_{VL} = \frac{V_o}{V_i} = \frac{R_E \| R_L}{R_E \| R_L + r_e}$$

$$Z_i = R_B \| Z_b$$

$$Z_b \cong \beta (R_E \| R_L)$$

$$Z_o \cong r_e$$

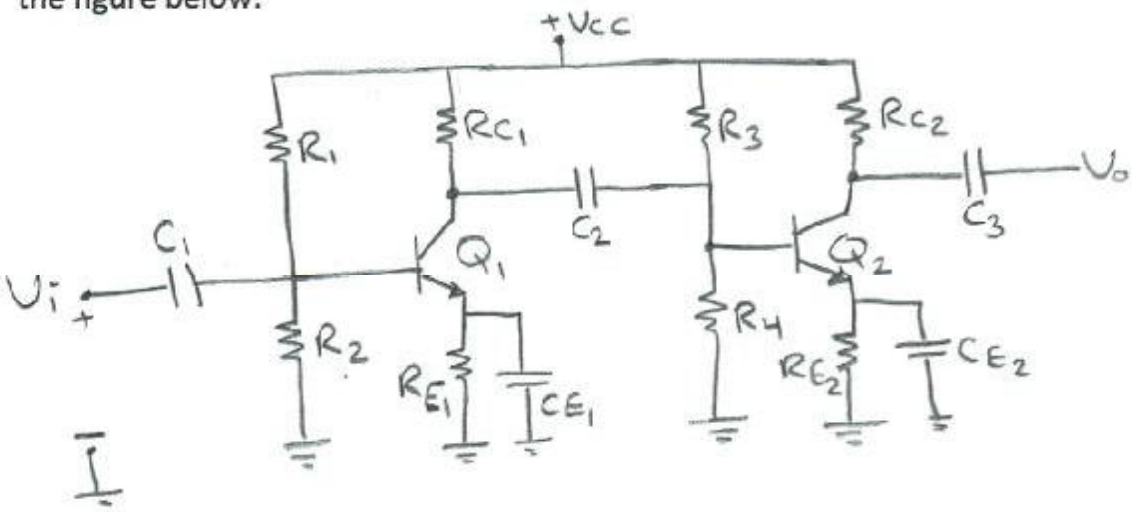
~~Second approach (two-port system approach):-~~

Cascade Configuration:

In the cascade configuration the output of one stage appears as the input for the following stage. The input impedance for the second stage is the load impedance for the first stage.

The total gain is the product of the gain of each stage including the loading effects of the following stage.

One popular connection of amplifier stages is the RC-Coupled amplifier shown in the figure below:



The coupling capacitors isolate the two stages from a dc viewpoint but acts as a short circuit equivalent for the ac response.

Example 5.15

Important Notes:

- The loaded voltage gain of an amplifier is always less than the no-load gain.
- The gain with a source resistance will always be less than that under loaded or unloaded conditions.

  $\therefore A_{VNL} > A_{VL} > A_{VS}$
- For a particular design, the larger the level of R_L, the greater is the level of the ac gain. As R_L gets larger A_{VL} approaches A_{VNL}.

If $R_L \rightarrow \infty$ $A_{VL} \cong A_{VNL}$.

- For a particular amplifier, the smaller the internal resistance of the signal source, the greater is the overall gain.

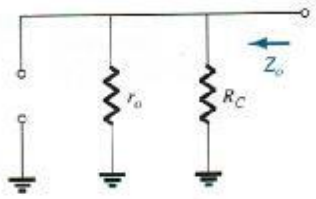


FIG. 5.23
Determining Z_o for the network of Fig. 5.22.

Z_o Recall that the output impedance of any system is defined as the impedance Z_o determined when $V_i = 0$. For Fig. 5.22, when $V_i = 0$, $I_i = I_b = 0$, resulting in an open-circuit equivalence for the current source. The result is the configuration of Fig. 5.23. We have

$$Z_o = R_C \| r_o \quad \text{ohms} \tag{5.3}$$

If $r_o \geq 10R_C$, the approximation $R_C \| r_o \cong R_C$ is frequently applied, and

$$Z_o \cong R_C \quad r_o \geq 10R_C \tag{5.4}$$

A_v The resistors r_o and R_C are in parallel, and

$$V_o = -\beta I_b (R_C \| r_o)$$

but

$$I_b = \frac{V_i}{\beta r_e}$$

so that

$$V_o = -\beta \left(\frac{V_i}{\beta r_e} \right) (R_C \| r_o)$$

and

$$A_v = \frac{V_o}{V_i} = -\frac{(R_C \| r_o)}{r_e} \tag{5.5}$$

If $r_o \geq 10R_C$, so that the effect of r_o can be ignored,

$$A_v = -\frac{R_C}{r_e} \quad r_o \geq 10R_C \tag{5.6}$$

Note the explicit absence of β in Eqs. (5.5) and (5.6), although we recognize that β must be utilized to determine r_e.

Phase Relationship The negative sign in the resulting equation for A_v reveals that a 180° phase shift occurs between the input and output signals, as shown in Fig. 5.24. The is a result of the fact that βI_b establishes a current through R_C that will result in a voltage across R_C, the opposite of that defined by V_o.

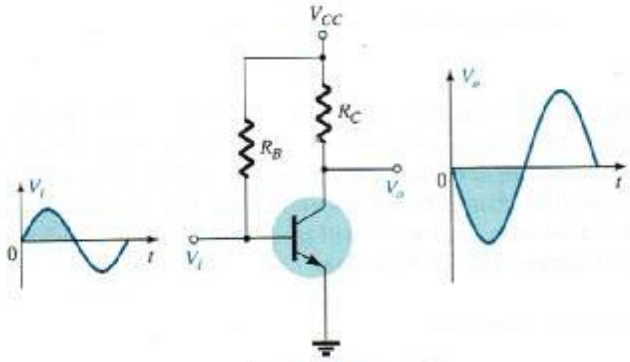


FIG. 5.24
Demonstrating the 180° phase shift between input and output waveforms.

EXAMPLE 5.1 For the network of Fig. 5.25:

a. Determine r_e.
b. Find Z_i (with $r_o = \infty\ \Omega$).

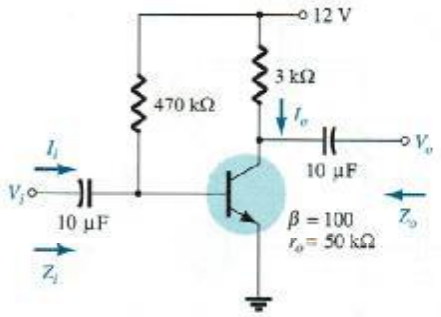


FIG. 5.25
Example 5.1.

c. Calculate Z_o (with $r_o = \infty\ \Omega$).
d. Determine A_v (with $r_o = \infty\ \Omega$).
e. Repeat parts (c) and (d) including $r_o = 50\ \text{k}\Omega$ in all calculations and compare results.

Solution:

a. DC analysis:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B} = \frac{12\ \text{V} - 0.7\ \text{V}}{470\ \text{k}\Omega} = 24.04\ \mu\text{A}$$

$$I_E = (\beta + 1)I_B = (101)(24.04\ \mu\text{A}) = 2.428\ \text{mA}$$

$$r_e = \frac{26\ \text{mV}}{I_E} = \frac{26\ \text{mV}}{2.428\ \text{mA}} = \mathbf{10.71\ \Omega}$$

b. $\beta r_e = (100)(10.71\ \Omega) = 1.071\ \text{k}\Omega$

$$Z_i = R_B \| \beta r_e = 470\ \text{k}\Omega \| 1.071\ \text{k}\Omega = \mathbf{1.07\ k\Omega}$$

c. $Z_o = R_C = \mathbf{3\ k\Omega}$

d. $$A_v = -\frac{R_C}{r_e} = -\frac{3\ \text{k}\Omega}{10.71\ \Omega} = \mathbf{-280.11}$$

e. $Z_o = r_o \| R_C = 50\ \text{k}\Omega \| 3\ \text{k}\Omega = \mathbf{2.83\ k\Omega}$ vs. $3\ \text{k}\Omega$

$$A_v = -\frac{r_o \| R_C}{r_e} = \frac{2.83\ \text{k}\Omega}{10.71\ \Omega} = \mathbf{-264.24}\ \text{vs.}\ -280.11$$

5.6 VOLTAGE-DIVIDER BIAS

The next configuration to be analyzed is the *voltage-divider* bias network of Fig. 5.26. Recall that the name of the configuration is a result of the voltage-divider bias at the input side to determine the dc level of V_B.

Substituting the r_e equivalent circuit results in the network of Fig. 5.27. Note the absence of R_E due to the low-impedance shorting effect of the bypass capacitor, C_E. That is, at the frequency (or frequencies) of operation, the reactance of the capacitor is so small compared to R_E that it is treated as a short circuit across R_E. When V_{CC} is set to zero, it places one end of R_1 and R_C at ground potential as shown in Fig. 5.27. In addition, note that R_1 and R_2 remain part of the input circuit, whereas R_C is part of the output circuit. The parallel combination of R_1 and R_2 is defined by

$$R' = R_1 \| R_2 = \frac{R_1 R_2}{R_1 + R_2} \tag{5.7}$$

Z_i From Fig. 5.27

$$Z_i = R' \| \beta r_e \tag{5.8}$$

For $r_o \geq 10R_C$,

$$A_v = \frac{V_o}{V_i} \cong -\frac{R_C}{r_e} \qquad r_o \geq 10R_C \qquad (5.12)$$

Phase Relationship The negative sign of Eq. (5.11) reveals a 180° phase shift between V_o and V_i.

EXAMPLE 5.2 For the network of Fig. 5.28, determine:

a. r_e.
b. Z_i.
c. Z_o ($r_o = \infty\ \Omega$).
d. A_v ($r_o = \infty\ \Omega$).
e. The parameters of parts (b) through (d) if $r_o = 50\ \text{k}\Omega$ and compare results.

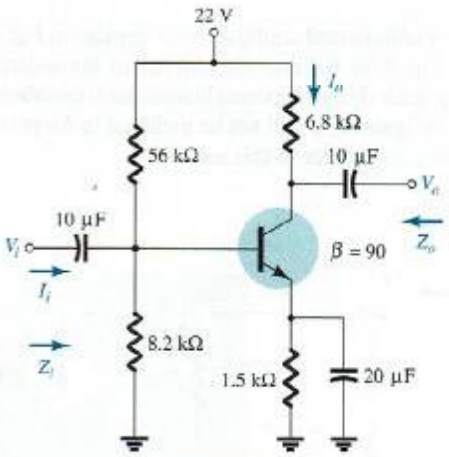


FIG. 5.28
Example 5.2.

Solution:

a. DC: Testing $\beta R_E > 10R_2$,

$$(90)(1.5\ \text{k}\Omega) > 10(8.2\ \text{k}\Omega)$$
$$135\ \text{k}\Omega \geq 82\ \text{k}\Omega\ (\textit{satisfied})$$

Using the approximate approach, we obtain

$$V_B = \frac{R_2}{R_1 + R_2} V_{CC} = \frac{(8.2\ \text{k}\Omega)(22\ \text{V})}{56\ \text{k}\Omega + 8.2\ \text{k}\Omega} = 2.81\ \text{V}$$
$$V_E = V_B - V_{BE} = 2.81\ \text{V} - 0.7\ \text{V} = 2.11\ \text{V}$$
$$I_E = \frac{V_E}{R_E} = \frac{2.11\ \text{V}}{1.5\ \text{k}\Omega} = 1.41\ \text{mA}$$
$$r_e = \frac{26\ \text{mV}}{I_E} = \frac{26\ \text{mV}}{1.41\ \text{mA}} = \mathbf{18.44\ \Omega}$$

b. $R' = R_1 \| R_2 = (56\ \text{k}\Omega) \| (8.2\ \text{k}\Omega) = 7.15\ \text{k}\Omega$
$Z_i = R' \| \beta r_e = 7.15\ \text{k}\Omega \| (90)(18.44\ \Omega) = 7.15\ \text{k}\Omega \| 1.66\ \text{k}\Omega$
$= \mathbf{1.35\ \text{k}\Omega}$

c. $Z_o = R_C = \mathbf{6.8\ \text{k}\Omega}$

d. $A_v = -\frac{R_C}{r_e} = -\frac{6.8\,\text{k}\Omega}{18.44\,\Omega} = \mathbf{-368.76}$

e. $Z_i = \mathbf{1.35\,k\Omega}$

$Z_o = R_C \| r_o = 6.8\,\text{k}\Omega \| 50\,\text{k}\Omega = \mathbf{5.98\,k\Omega}$ vs. $6.8\,\text{k}\Omega$

$A_v = -\frac{R_C \| r_o}{r_e} = -\frac{5.98\,\text{k}\Omega}{18.44\,\Omega} = \mathbf{-324.3}$ vs. -368.76

There was a measurable difference in the results for Z_o and A_v, because the condition $r_o \geq 10R_C$ was *not* satisfied.

5.7 CE EMITTER-BIAS CONFIGURATION

The networks examined in this section include an emitter resistor that may or may not be bypassed in the ac domain. We first consider the unbypassed situation and then modify the resulting equations for the bypassed configuration.

Unbypassed

The most fundamental of unbypassed configurations appears in Fig. 5.29. The r_e equivalent model is substituted in Fig. 5.30, but note the absence of the resistance r_o. The effect of r_o is to make the analysis a great deal more complicated, and considering the fact that in most situations its effect can be ignored, it will not be included in the present analysis. However, the effect of r_o will be discussed later in this section.

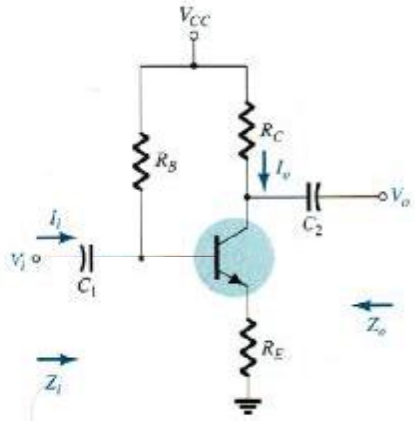


FIG. 5.29
CE emitter-bias configuration.

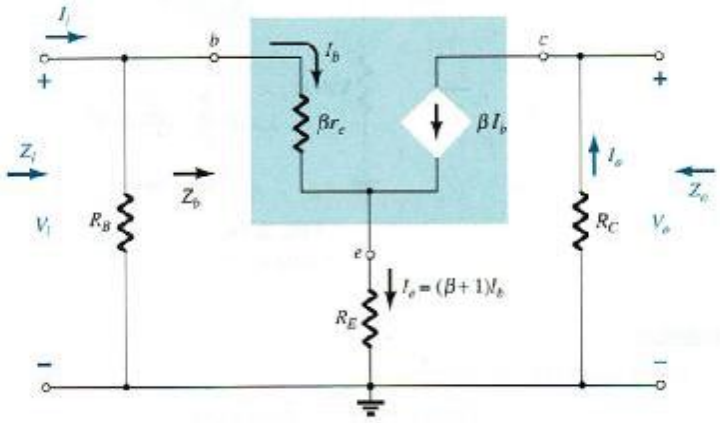


FIG. 5.30
Substituting the r_e equivalent circuit into the ac equivalent network of Fig. 5.29.

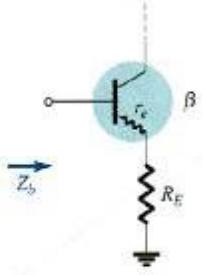


FIG. 5.31
Defining the input impedance of a transistor with an unbypassed emitter resistor.

Applying Kirchhoff's voltage law to the input side of Fig. 5.30 results in

$$V_i = I_b\beta r_e + I_e R_E$$

or

$$V_i = I_b\beta r_e + (\beta + 1)I_b R_E$$

and the input impedance looking into the network to the right of R_B is

$$Z_b = \frac{V_i}{I_b} = \beta r_e + (\beta + 1)R_E$$

The result as displayed in Fig. 5.31 reveals that the input impedance of a transistor with an unbypassed resistor R_E is determined by

$$\boxed{Z_b = \beta r_e + (\beta + 1)R_E} \qquad \textbf{(5.13)}$$

For $r_o \geq 10R_C$,

$$A_v = \frac{V_o}{V_i} \cong -\frac{\beta R_C}{Z_b} \qquad r_o \geq 10R_C \qquad (5.26)$$

as obtained earlier.

Bypassed

If R_E of Fig. 5.29 is bypassed by an emitter capacitor C_E, the complete r_e equivalent model can be substituted, resulting in the same equivalent network as Fig. 5.22. Equations (5.1) to (5.6) are therefore applicable.

EXAMPLE 5.3 For the network of Fig. 5.32, without C_E (unbypassed), determine:

a. r_e.
b. Z_i.
c. Z_o.
d. A_v.

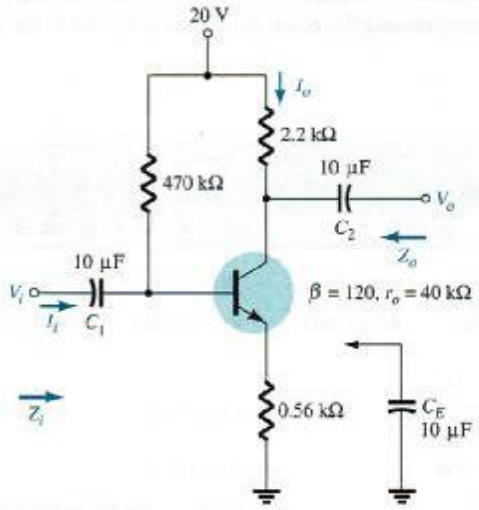


FIG. 5.32
Example 5.3.

Solution:

a. DC:

$$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E} = \frac{20\text{ V} - 0.7\text{ V}}{470\text{ k}\Omega + (121)0.56\text{ k}\Omega} = 35.89\ \mu\text{A}$$

$$I_E = (\beta + 1)I_B = (121)(35.89\ \mu\text{A}) = 4.34\text{ mA}$$

and $$r_e = \frac{26\text{ mV}}{I_E} = \frac{26\text{ mV}}{4.34\text{ mA}} = \mathbf{5.99\ \Omega}$$

b. Testing the condition $r_o \geq 10(R_C + R_E)$, we obtain

$$40\text{ k}\Omega \geq 10(2.2\text{ k}\Omega + 0.56\text{ k}\Omega)$$

$$40\text{ k}\Omega \geq 10(2.76\text{ k}\Omega) = 27.6\text{ k}\Omega\ (\textit{satisfied})$$

Therefore,

$$Z_b \cong \beta(r_e + R_E) = 120(5.99\ \Omega + 560\ \Omega)$$

$$= 67.92\text{ k}\Omega$$

and

$$Z_i = R_B \| Z_b = 470\text{ k}\Omega \| 67.92\text{ k}\Omega$$

$$= \mathbf{59.34\text{ k}\Omega}$$

c. $Z_o = R_C = \mathbf{2.2\,k\Omega}$

d. $r_o \geq 10R_C$ is satisfied. Therefore,

$$A_v = \frac{V_o}{V_i} \cong -\frac{\beta R_C}{Z_b} = -\frac{(120)(2.2\,\text{k}\Omega)}{67.92\,\text{k}\Omega}$$

$$= \mathbf{-3.89}$$

compared to -3.93 using Eq. (5.20): $A_v \cong -R_C/R_E$.

Mathcad

The lengthy equations resulting from the analysis of the CE emitter-bias configuration demonstrate the value of becoming proficient in the use of the Mathcad software package.

Priorities do not permit a detailed description of each step of the process, but a few general comments can be made. First, all the parameters of the network that will appear in the equations must be defined as shown in Fig. 5.33. Next, the equations for each of the desired quantities are entered, being very careful to include parentheses in the proper places to ensure that the resulting equation is correct. Actually, more parentheses appear than necessary, but an effort was made to make the equations look as much like those in the text as possible. After each equation is defined, its value can be determined by simply entering the variable name again and pressing the equal sign. This is shown to the right of each equation

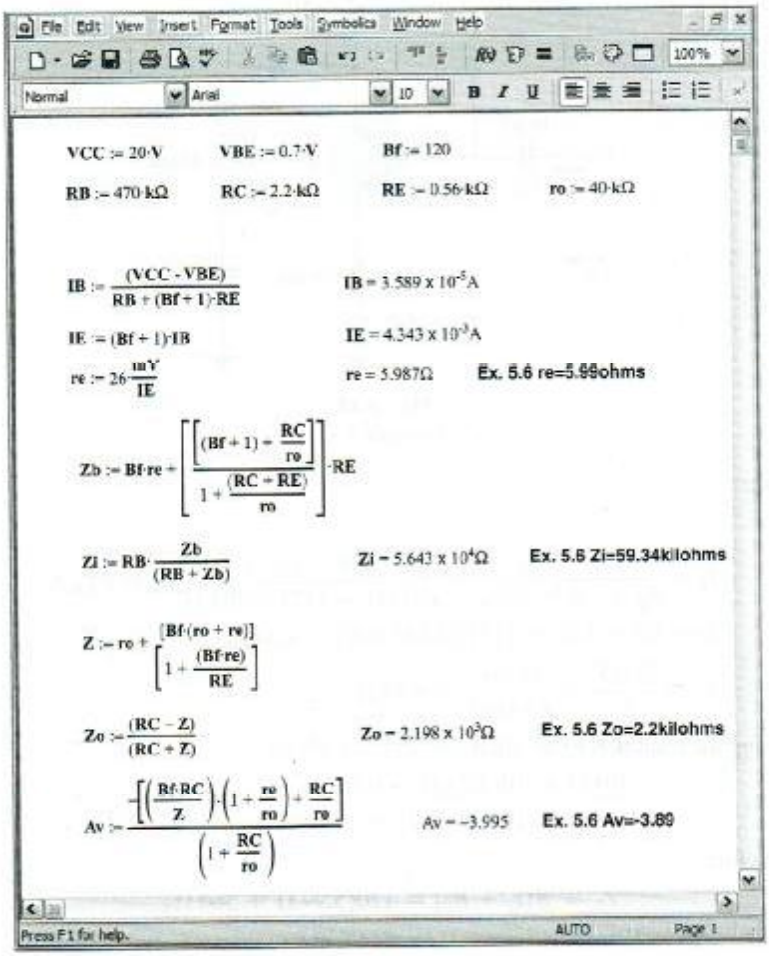


FIG. 5.33

Network parameters and equations for Example 5.3.

at a level just below the defining equation. For the base current, for example, once **IB** is entered and the equal sign pressed, the base current of 35.89 μA will appear. Note as you progress down the page that as a variable is determined, it can be used in the equations to follow. In fact, it is a necessary sequence if the continuing line of equations is to have the specific numbers to deal with.

For each of the quantities calculated, a text message is added to permit a comparison with the results of Example 5.3. There is excellent correspondence between results when one considers that a number of approximations were used in Example 5.3. The largest difference occurs for the input impedance, which has a lengthy equation for **Zb**. That difference is reflected in the current gain, which has a greater difference than that obtained for the output impedance and voltage gain.

The real beauty of having entered all these equations properly is that the file can be saved and recalled at any time. As the parameters appearing on the first two lines are changed, all the quantities on the following lines will be recalculated—there is no need to reenter any of the equations, and this sequence even does the dc analysis before determining the ac response.

EXAMPLE 5.4 Repeat the analysis of Example 5.3 with C_E in place.

Solution:

a. The dc analysis is the same, and $r_e = 5.99\ \Omega$.

b. R_E is "shorted out" by C_E for the ac analysis. Therefore,

$$Z_i = R_B \| Z_b = R_B \| \beta r_e = 470\,\text{k}\Omega \| (120)(5.99\ \Omega)$$
$$= 470\,\text{k}\Omega \| 718.8\ \Omega \cong \mathbf{717.70\ \Omega}$$

c. $Z_o = R_C = \mathbf{2.2\,k\Omega}$

d. $$A_v = -\frac{R_C}{r_e}$$
$$= -\frac{2.2\,\text{k}\Omega}{5.99\ \Omega} = \mathbf{-367.28}\ \text{(a significant increase)}$$

EXAMPLE 5.5 For the network of Fig. 5.34 (with C_E unconnected), determine (using appropriate approximations):

a. r_e.
b. Z_i.
c. Z_o.
d. A_v.

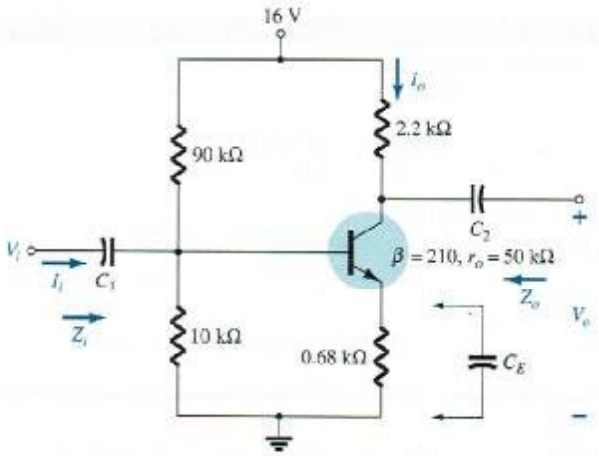


FIG. 5.34
Example 5.5.

Solution:

a. Testing $\beta R_E > 10R_2$,

$$(210)(0.68\,\text{k}\Omega) > 10(10\,\text{k}\Omega)$$
$$142.8\,\text{k}\Omega > 100\,\text{k}\Omega \ (\textit{satisfied})$$

we have

$$V_B = \frac{R_2}{R_1 + R_2} V_{CC} = \frac{10\,\text{k}\Omega}{90\,\text{k}\Omega + 10\,\text{k}\Omega}(16\,\text{V}) = 1.6\,\text{V}$$
$$V_E = V_B - V_{BE} = 1.6\,\text{V} - 0.7\,\text{V} = 0.9\,\text{V}$$
$$I_E = \frac{V_E}{R_E} = \frac{0.9\,\text{V}}{0.68\,\text{k}\Omega} = 1.324\,\text{mA}$$
$$r_e = \frac{26\,\text{mV}}{I_E} = \frac{26\,\text{mV}}{1.324\,\text{mA}} = \mathbf{19.64\,\Omega}$$

b. The ac equivalent circuit is provided in Fig. 5.35. The resulting configuration is different from Fig. 5.30 only by the fact that now

$$R_B = R' = R_1 \| R_2 = 9\,\text{k}\Omega$$

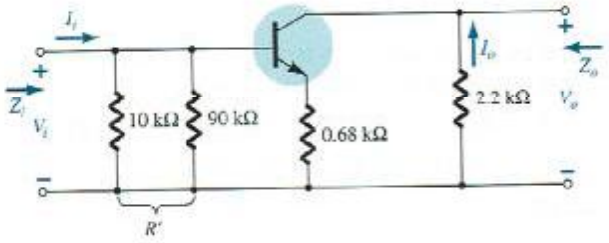


FIG. 5.35
The ac equivalent circuit of Fig. 5.34.

The testing conditions of $r_o \geq 10(R_C + R_E)$ and $r_o \geq 10R_C$ are both satisfied. Using the appropriate approximations yields

$$Z_b \cong \beta R_E = 142.8\,\text{k}\Omega$$
$$Z_i = R_B \| Z_b = 9\,\text{k}\Omega \| 142.8\,\text{k}\Omega$$
$$= \mathbf{8.47\,\text{k}\Omega}$$

c. $Z_o = R_C = \mathbf{2.2\,\text{k}\Omega}$

d. $A_v = -\frac{R_C}{R_E} = -\frac{2.2\,\text{k}\Omega}{0.68\,\text{k}\Omega} = \mathbf{-3.24}$

EXAMPLE 5.6 Repeat Example 5.5 with C_E in place.

Solution:

a. The dc analysis is the same, and $r_e = \mathbf{19.64\,\Omega}$.

b. $Z_b = \beta r_e = (210)(19.64\,\Omega) \cong 4.12\,\text{k}\Omega$

$$Z_i = R_B \| Z_b = 9\,\text{k}\Omega \| 4.12\,\text{k}\Omega$$
$$= \mathbf{2.83\,\text{k}\Omega}$$

c. $Z_o = R_C = \mathbf{2.2\,\text{k}\Omega}$

d. $A_v = -\frac{R_C}{r_e} = -\frac{2.2\,\text{k}\Omega}{19.64\,\Omega} = \mathbf{-112.02}$ (a significant increase)

Another variation of an emitter-bias configuration is shown in Fig. 5.36. For the dc analysis, the emitter resistance is $R_{E_1} + R_{E_2}$, whereas for the ac analysis, the resistor R_E in the equations above is simply R_{E_1} with R_{E_2} bypassed by C_E.

But $$Z_b \cong \beta(r_e + R_E)$$

so that $$A_v \cong \frac{\beta R_E}{\beta(r_e + R_E)}$$

and $$\boxed{A_v \cong \frac{R_E}{r_e + R_E}} \quad r_o \geq 10R_E \qquad (5.41)$$

EXAMPLE 5.7 For the emitter-follower network of Fig. 5.40, determine:

a. r_e.
b. Z_i.
c. Z_o.
d. A_v.
e. Repeat parts (b) through (d) with $r_o = 25\,\text{k}\Omega$ and compare results.

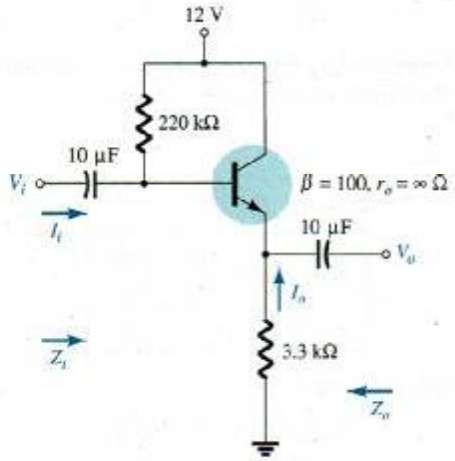


FIG. 5.40
Example 5.7.

Solution:

a. $$I_B = \frac{V_{CC} - V_{BE}}{R_B + (\beta + 1)R_E}$$
$$= \frac{12\,\text{V} - 0.7\,\text{V}}{220\,\text{k}\Omega + (101)3.3\,\text{k}\Omega} = 20.42\,\mu\text{A}$$
$$I_E = (\beta + 1)I_B$$
$$= (101)(20.42\,\mu\text{A}) = 2.062\,\text{mA}$$
$$r_e = \frac{26\,\text{mV}}{I_E} = \frac{26\,\text{mV}}{2.062\,\text{mA}} = \mathbf{12.61\,\Omega}$$

b. $$Z_b = \beta r_e + (\beta + 1)R_E$$
$$= (100)(12.61\,\Omega) + (101)(3.3\,\text{k}\Omega)$$
$$= 1.261\,\text{k}\Omega + 333.3\,\text{k}\Omega$$
$$= 334.56\,\text{k}\Omega \cong \beta R_E$$
$$Z_i = R_B \| Z_b = 220\,\text{k}\Omega \| 334.56\,\text{k}\Omega$$
$$= \mathbf{132.72\,k\Omega}$$

c. $$Z_o = R_E \| r_e = 3.3\,\text{k}\Omega \| 12.61\,\Omega$$
$$= \mathbf{12.56\,\Omega} \cong r_e$$

d. $$A_v = \frac{V_o}{V_i} = \frac{R_E}{R_E + r_e} = \frac{3.3\,\text{k}\Omega}{3.3\,\text{k}\Omega + 12.61\,\Omega}$$
$$= \mathbf{0.996} \cong \mathbf{1}$$

e. Checking the condition $r_o \geq 10R_E$, we have

$$25\,\text{k}\Omega \geq 10(3.3\,\text{k}\Omega) = 33\,\text{k}\Omega$$

which is *not* satisfied. Therefore,

$$Z_i = \beta r_e + \frac{(\beta + 1)R_E}{1 + \frac{R_E}{r_o}} = (100)(12.61\,\Omega) + \frac{(100 + 1)3.3\,\text{k}\Omega}{1 + \frac{3.3\,\text{k}\Omega}{25\,\text{k}\Omega}}$$

$$= 1.261\,\text{k}\Omega + 294.43\,\text{k}\Omega$$

$$= 295.7\,\text{k}\Omega$$

with $Z_i = R_B \| Z_b = 220\,\text{k}\Omega \| 295.7\,\text{k}\Omega$

$$= \mathbf{126.15\,k\Omega} \text{ vs. } 132.72\,\text{k}\Omega \quad \text{obtained earlier}$$

$$Z_o = R_L \| r_e = \mathbf{12.56\,\Omega} \quad \text{as obtained earlier}$$

$$A_v = \frac{(\beta + 1)R_E/Z_b}{\left[1 + \frac{R_E}{r_o}\right]} = \frac{(100 + 1)(3.3\,\text{k}\Omega)/295.7\,\text{k}\Omega}{\left[1 + \frac{3.3\,\text{k}\Omega}{25\,\text{k}\Omega}\right]}$$

$$= \mathbf{0.996} \cong 1$$

matching the earlier result.

In general, therefore, even though the condition $r_o \geq 10R_E$ is not satisfied, the results for Z_i and A_v are the same, with Z_i only slightly less. The results suggest that for most applications a good approximation for the actual results can be obtained by simply ignoring the effects of r_o for this configuration.

The network of Fig. 5.41 is a variation of the network of Fig. 5.37, which employs a voltage-divider input section to set the bias conditions. Equations (5.27) to (5.30) are changed only by replacing R_B by $R' = R_1 \| R_2$.

The network of Fig. 5.42 also provides the input/output characteristics of an emitter-follower, but includes a collector resistor R_C. In this case R_B is again replaced by the parallel combination of R_1 and R_2. The input impedance Z_i and output impedance Z_o are unaffected by R_C because it is not reflected into the base or emitter equivalent networks. In fact, the only effect of R_C is to determine the Q-point of operation.

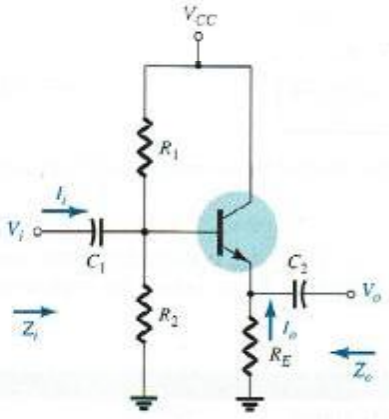


FIG. 5.41
Emitter-follower configuration with a voltage-divider biasing arrangement.

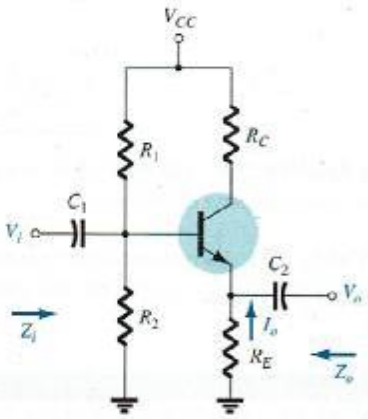


FIG. 5.42
Emitter-follower configuration with a collector resistor R_C.

5.9 COMMON-BASE CONFIGURATION

The common-base configuration is characterized as having a relatively low input and a high output impedance and a current gain less than 1. The voltage gain, however, can be quite large. The standard configuration appears in Fig. 5.43, with the common-base r_e equivalent model substituted in Fig. 5.44. The transistor output impedance r_o is not included for the

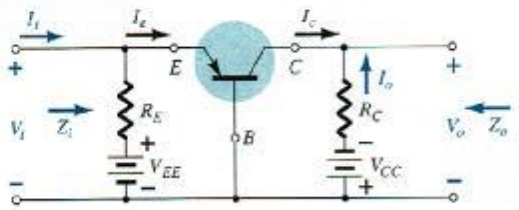


FIG. 5.43
Common-base configuration.

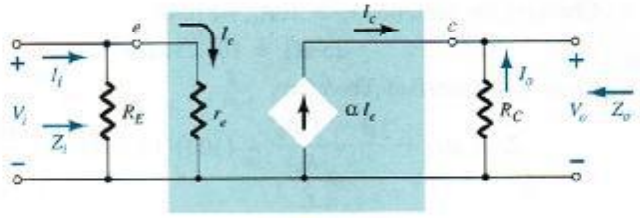


FIG. 5.44
Substituting the r_e equivalent circuit into the ac equivalent network of Fig. 5.45.

common-base configuration because it is typically in the megohm range and can be ignored in parallel with the resistor R_C.

Z_i

$$Z_i = R_E \| r_e \tag{5.42}$$

Z_o

$$Z_o = R_C \tag{5.43}$$

A_v

$$V_o = -I_o R_C = -(-I_c)R_C = \alpha I_e R_C$$

with $$I_e = \frac{V_i}{r_e}$$

so that $$V_o = \alpha\left(\frac{V_i}{r_e}\right)R_C$$

and

$$A_v = \frac{V_o}{V_i} = \frac{\alpha R_C}{r_e} \cong \frac{R_C}{r_e} \tag{5.44}$$

A_i Assuming that $R_E \gg r_e$ yields

$$I_e = I_i$$

and $$I_o = -\alpha I_e = -\alpha I_i$$

with

$$A_i = \frac{I_o}{I_i} = -\alpha \cong -1 \tag{5.45}$$

Phase Relationship The fact that A_v is a positive number shows that V_o and V_i are in phase for the common-base configuration.

Effect of r_o For the common-base configuration, $r_o = 1/h_{ob}$ is typically in the megohm range and sufficiently larger than the parallel resistance R_C to permit the approximation $r_o \| R_C \cong R_C$.

EXAMPLE 5.8 For the network of Fig. 5.45, determine:

a. r_e.
b. Z_i.
c. Z_o.
d. A_v.
e. A_i.

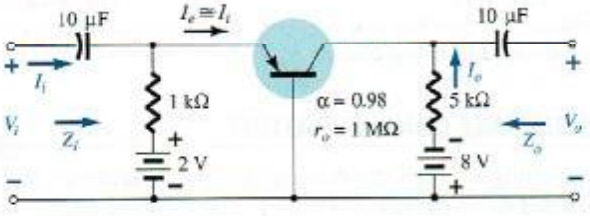


FIG. 5.45
Example 5.8.

Solution:

a. $I_E = \dfrac{V_{EE} - V_{BE}}{R_E} = \dfrac{2\text{ V} - 0.7\text{ V}}{1\text{ k}\Omega} = \dfrac{1.3\text{ V}}{1\text{ k}\Omega} = 1.3\text{ mA}$

$r_e = \dfrac{26\text{ mV}}{I_E} = \dfrac{26\text{ mV}}{1.3\text{ mA}} = \mathbf{20\ \Omega}$

b. $Z_i = R_E | r_e = 1\text{ k}\Omega \| 20\ \Omega$

$= \mathbf{19.61\ \Omega} \cong r_e$

c. $Z_o = R_C = \mathbf{5\text{ k}\Omega}$

d. $A_v \cong \dfrac{R_C}{r_e} = \dfrac{5\text{ k}\Omega}{20\ \Omega} = \mathbf{250}$

e. $A_i = \mathbf{-0.98} \cong -1$

5.10 COLLECTOR FEEDBACK CONFIGURATION

The collector feedback network of Fig. 5.46 employs a feedback path from collector to base to increase the stability of the system as discussed in Section 4.6. However, the simple maneuver of connecting a resistor from base to collector rather than base to dc supply has a significant effect on the level of difficulty encountered when analyzing the network.

Some of the steps to be performed below are the result of experience working with such configurations. It is not expected that a new student of the subject would choose the sequence of steps described below without taking a wrong step or two. Substituting the equivalent circuit and redrawing the network results in the configuration of Fig. 5.47. The effects of a transistor output resistance r_o will be discussed later in the section.

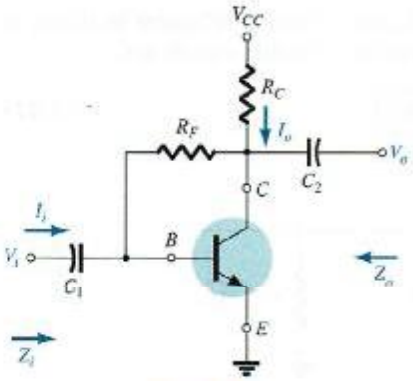


FIG. 5.46
Collector feedback configuration.

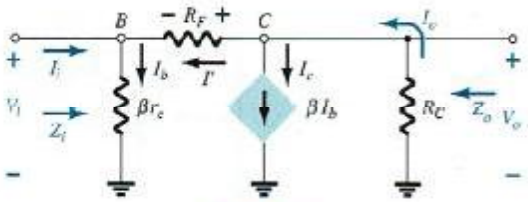


FIG. 5.47
Substituting the r_e equivalent circuit into the ac equivalent network of Fig. 5.46.

Z_i

$$I' = \frac{V_o - V_i}{R_F}$$

with $$V_o = -I_o R_C$$

and $$I_o = \beta I_b + I'$$

Because βI_b is normally much larger than I',

$$I_o \cong \beta I_b$$

and $$V_o = -(\beta I_b)R_C = -\beta I_b R_C$$

but $$I_b = \frac{V_i}{\beta r_e}$$

and $$V_o = -\beta\left(\frac{V_i}{\beta r_e}\right)R_C = -\frac{R_C}{r_e}V_i$$

EXAMPLE 5.11 Using the parameter values for the fixed-bias configuration of Example 5.1 with an applied load of 4.7 kΩ and a source resistance of 0.3 kΩ, determine the following and compare to the no-load values:

a. A_{v_L}.
b. A_{v_s}.
c. Z_i.
d. Z_o.

Solution:

a. Eq. (5.70): $A_{v_L} = -\dfrac{R_C \| R_L}{r_e} = -\dfrac{3\,\text{k}\Omega \| 4.7\,\text{k}\Omega}{10.71\,\Omega} = -\dfrac{1.831\,\text{k}\Omega}{10.71\,\Omega} = \mathbf{-170.98}$

which is significantly less than the no-load gain of −280.11.

b. Eq. (5.73): $A_{v_s} = \dfrac{Z_i}{Z_i + R_s} A_{v_L}$

With $Z_i = 1.07\,\text{k}\Omega$ from Example 5.1, we have

$$A_{v_s} = \frac{1.07\,\text{k}\Omega}{1.07\,\text{k}\Omega + 0.3\,\text{k}\Omega}(-170.98) = \mathbf{-133.54}$$

which again is significantly less than $A_{v_{NL}}$ or A_{v_L}.

c. $Z_i = \mathbf{1.07\,k\Omega}$ as obtained for the no-load situation.

d. $Z_o = R_C = \mathbf{3\,k\Omega}$ as obtained for the no-load situation.

The example clearly demonstrates that $A_{v_{NL}} > A_{v_L} > A_{v_s}$.

For the voltage-divider configuration of Fig. 5.58 with an applied load and series source resistor the ac equivalent network is as shown in Fig. 5.59.

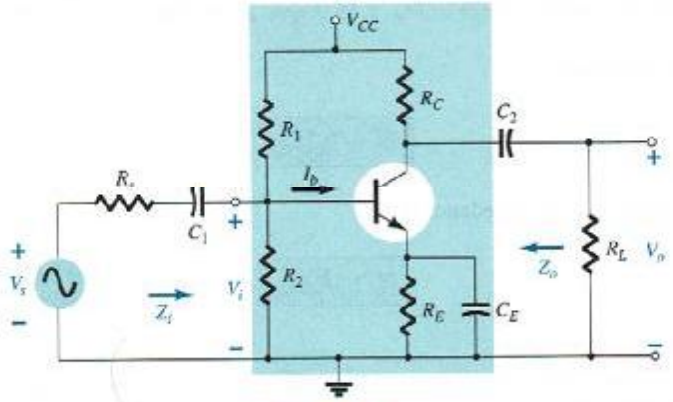


FIG. 5.58
Voltage-divider bias configuration with R_s and R_L.

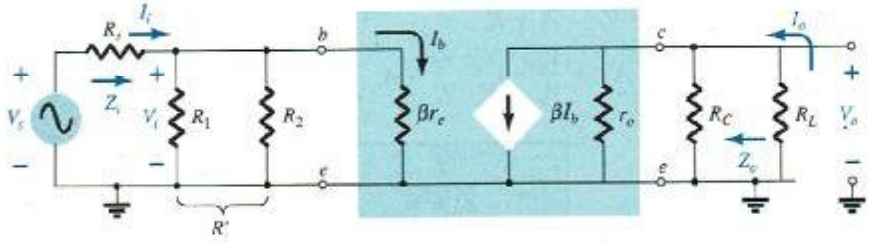


FIG. 5.59
Substituting the r_e equivalent circuit into the ac equivalent network of Fig. 5.58.

Eq. (5.85): $$A_{v_s} = \frac{Z_i}{Z_i + R_s} A_{v_f} = \frac{(10\,\text{k}\Omega)(101.20)}{10\,\text{k}\Omega + 1\,\text{k}\Omega}$$
$$= \mathbf{92}$$

c. Eq. (5.94): $$A_{i_f} = -A_{v_f}\frac{Z_i}{R_L} = -(101.20)\left(\frac{10\,\text{k}\Omega}{8.2\,\text{k}\Omega}\right)$$
$$= \mathbf{-123.41}$$

d. Eq. (5.85): $$V_i = \frac{Z_{i_{CB}}}{Z_{i_{CB}} + R_s} V_s = \frac{26\,\Omega}{26\,\Omega + 1\,\text{k}\Omega} V_s = 0.025\,V_s$$

and $$\frac{V_i}{V_s} = 0.025 \quad \text{with} \quad \frac{V_o}{V_i} = 147.97 \quad \text{from above}$$

and $$A_{v_s} = \frac{V_o}{V_s} = \frac{V_i}{V_s}\cdot\frac{V_o}{V_i} = (0.025)(147.97) = \mathbf{3.7}$$

In total, therefore, the gain is about 25 times greater with the emitter-follower configuration to draw the signal to the amplifier stages. Note, however, that it is also important that the output impedance of the first stage is relatively close to the input impedance of the second stage, otherwise the signal would have been "lost" again by the voltage-divider action.

RC-Coupled BJT Amplifiers

One popular connection of amplifier stages is the *RC*-coupled variety shown in Fig. 5.71 in the next example. The name is derived from the capacitive coupling capacitor C_c and the fact that the load on the first stage is an *RC* combination. The coupling capacitor isolates the two stages from a dc viewpoint but acts as a short-circuit equivalent for the ac response. The input impedance of the second stage acts as a load on the first stage, permitting the same approach to the analysis as described in the last two sections.

EXAMPLE 5.15

a. Calculate the no-load voltage gain and output voltage of the *RC*-coupled transistor amplifiers of Fig. 5.71.
b. Calculate the overall gain and output voltage if a 4.7 kΩ load is applied to the second stage, and compare to the results of part (a).
c. Calculate the input impedance of the first stage and the output impedance of the second stage.

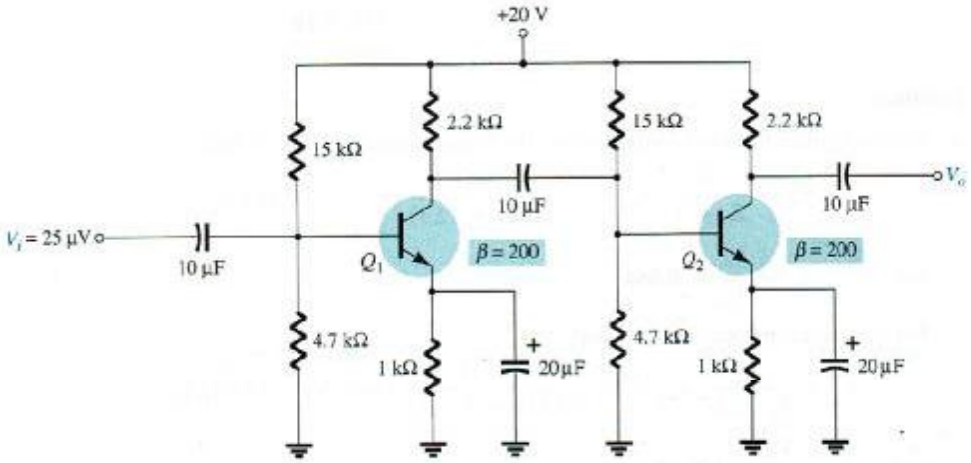


FIG. 5.71
RC-coupled BJT amplifier for Example 5.15.

Solution:

a. The dc bias analysis results in the following for each transistor:

$$V_B = 4.7\,\text{V}, \quad V_E = 4.0\,\text{V}, \quad V_C = 11\,\text{V}, \quad I_E = 4.0\,\text{mA}$$

At the bias point,

$$r_e = \frac{26\text{ mV}}{I_E} = \frac{26\text{ mV}}{4\text{ mA}} = 6.5\ \Omega$$

The loading of the second stage is

$$Z_{i_2} = R_1 \| R_2 \| \beta r_e$$

which results in the following gain for the first stage:

$$A_{v_1} = -\frac{R_C \| (R_1 \| R_2 \| \beta r_e)}{r_e}$$

$$= -\frac{(2.2\text{ k}\Omega) \| [15\text{ k}\Omega \| 4.7\text{ k}\Omega \| (200)(6.5\ \Omega)]}{6.5\ \Omega}$$

$$= -\frac{665.2\ \Omega}{6.5\ \Omega} = -102.3$$

For the unloaded second stage the gain is

$$A_{v_{2(\text{NL})}} = -\frac{R_C}{r_e} = -\frac{2.2\text{ k}\Omega}{6.5\ \Omega} = -338.46$$

resulting in an overall gain of

$$A_{v_{T(\text{NL})}} = A_{v_1} A_{v_{2(\text{NL})}} = (-102.3)(-338.46) \cong \mathbf{34.6 \times 10^3}$$

The output voltage is then

$$V_o = A_{v_{T(\text{NL})}} V_i = (34.6 \times 10^3)(25\ \mu\text{V}) \cong \mathbf{865\text{ mV}}$$

b. The overall gain with the 10-kΩ load applied is

$$A_{v_1} = \frac{V_o}{V_i} = \frac{R_L}{R_L + Z_o} A_{v_{T(\text{NL})}} = \frac{4.7\text{ k}\Omega}{4.7\text{ k}\Omega + 2.2\text{ k}\Omega}(34.6 \times 10^3) \cong \mathbf{23.6 \times 10^3}$$

which is considerably less than the unloaded gain because R_L is relatively close to R_C.

$$V_o = A_{v_T} V_i$$

$$= (23.6 \times 10^3)(25\ \mu\text{V})$$

$$= \mathbf{590\text{ mV}}$$

c. The input impedance of the first stage is

$$Z_{i_1} = R_1 \| R_2 \| \beta r_e = 4.7\text{ k}\Omega \| 15\text{ k}\Omega \| (200)(6.5\ \Omega) = \mathbf{953.6\ \Omega}$$

whereas the output impedance for the second stage is

$$Z_{o_2} = R_C = \mathbf{2.2\text{ k}\Omega}$$

Cascode Connection

The cascode configuration has one of two configurations. In each case the collector of the leading transistor is connected to the emitter of the following transistor. One possible arrangement appears in Fig. 5.72; the second is shown in Fig. 5.73 in the following example.

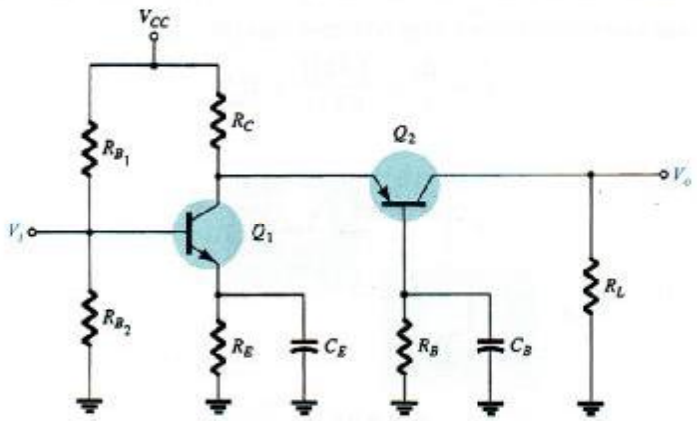


FIG. 5.72
Cascode configuration.

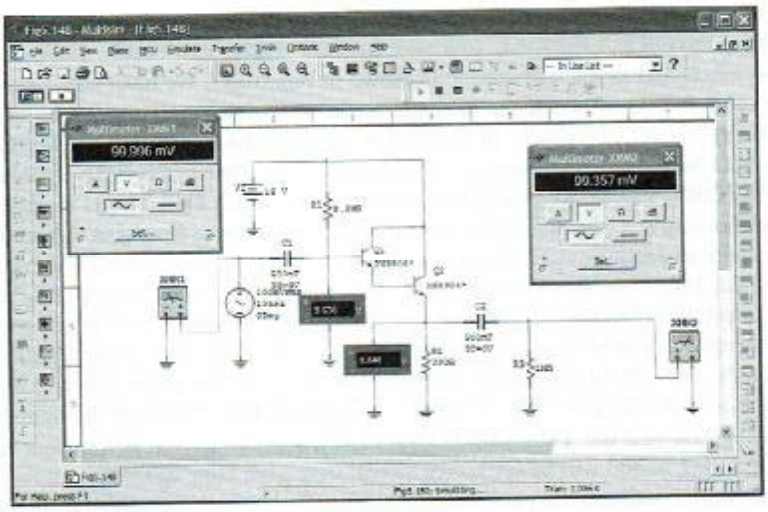


FIG. 5.148
Network of Example. 5.9 redrawn using Multisim.

PROBLEMS

**Note:* Asterisks indicate more difficult problems.

5.2 Amplification in the AC Domain

1. a. What is the expected amplification of a BJT transistor amplifier if the dc supply is set to zero volts?
   b. What will happen to the output ac signal if the dc level is insufficient? Sketch the effect on the waveform.
   c. What is the conversion efficiency of an amplifier in which the effective value of the current through a 2.2-kΩ load is 5 mA and the drain on the 18-V dc supply is 3.8 mA?
2. Can you think of an analogy that would explain the importance of the dc level on the resulting ac gain?

5.3 BJT Transistor Modeling

3. What is the reactance of a 10-μF capacitor at a frequency of 1 kHz? For networks in which the resistor levels are typically in the kilohm range, is it a good assumption to use the short-circuit equivalence for the conditions just described? How about at 100 kHz?
4. Given the common-base configuration of Fig. 5.149, sketch the ac equivalent using the notation for the transistor model appearing in Fig. 5.7.

5.4 The r_e Transistor Model

5. For the common-base configuration of Fig. 5.18, an ac signal of 10 mV is applied, resulting in an ac emitter current of 0.5 mA. If $\alpha = 0.980$, determine:
   a. Z_i.
   b. V_o if $R_L = 1.2\ \text{k}\Omega$.
   c. $A_v = V_o/V_i$.
   d. Z_o with $r_o = \infty\ \Omega$.
   e. $A_i = I_o/I_i$.
   f. I_b.

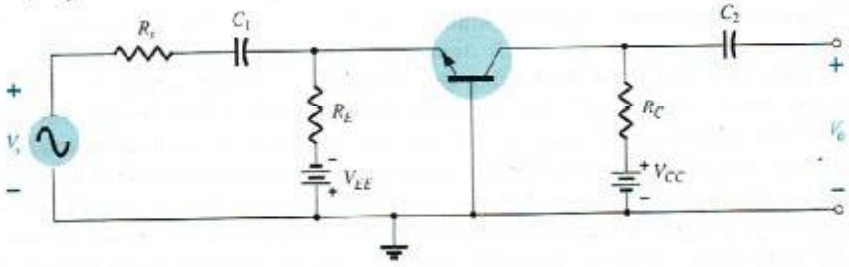


FIG. 5.149
Problem 4.

6. For the common-base configuration of Fig. 5.18, the dc emitter current is 3.2 mA and α is 0.99. Determine the following if the applied voltage is 48 mV and the load is 2.2 kΩ.
   a. r_e.
   b. Z_i.
   c. I_c.
   d. V_o.
   e. A_v.
   f. I_b.
7. Using the model of Fig. 5.16, determine the following for a common-emitter amplifier if $\beta = 80$, $I_E(\text{dc}) = 2\text{ mA}$, and $r_o = 40\text{ k}\Omega$.
   a. Z_i.
   b. I_b.
   c. $A_i = I_o/I_i = I_L/I_b$ if $R_L = 1.2\text{ k}\Omega$.
   d. A_v if $R_L = 1.2\text{ k}\Omega$.
8. The input impedance to a common-emitter transistor amplifier is 1.2 kΩ with $\beta = 140$, $r_o = 50\text{ k}\Omega$, and $R_L = 2.7\text{ k}\Omega$. Determine:
   a. r_e.
   b. I_b if $V_i = 30\text{ mV}$.
   c. I_c.
   d. $A_i = I_o/I_i = I_L/I_b$.
   e. $A_v = V_o/V_i$.

5.5 Common-Emitter Fixed-Bias Configuration

9. For the network of Fig. 5.150:
   a. Determine Z_i and Z_o.
   b. Find A_v.
   c. Repeat part (a) with $r_o = 20\text{ k}\Omega$.
   d. Repeat part (b) with $r_o = 20\text{ k}\Omega$.
10. For the network of Fig. 5.151, determine V_{CC} for a voltage gain of $A_v = -200$.

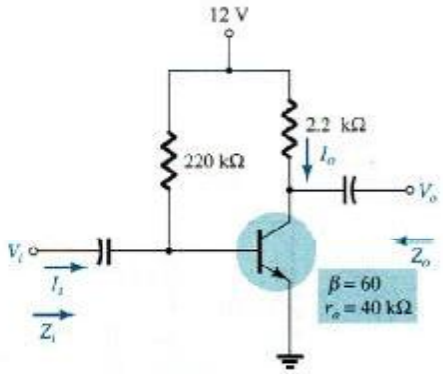


FIG. 5.150
Problem 9.

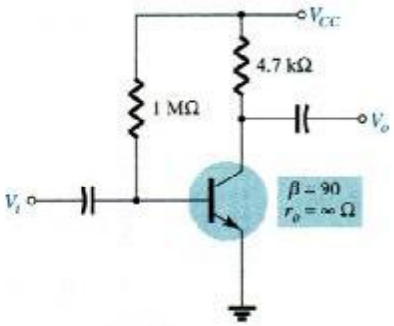


FIG. 5.151
Problem 10.

*11. For the network of Fig. 5.152:
   a. Calculate I_B, I_C, and r_e.
   b. Determine Z_i and Z_o.
   c. Calculate A_v.
   d. Determine the effect of $r_o = 30\text{ k}\Omega$ on A_v.

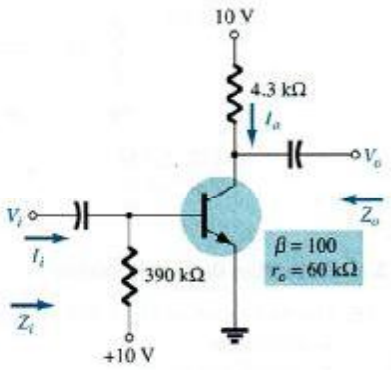


FIG. 5.152
Problem 11.

5.6 Voltage-Divider Bias

12. For the network of Fig. 5.153:
    a. Determine r_e.
    b. Calculate Z_i and Z_o.
    c. Find A_v.
    d. Repeat parts (b) and (c) with $r_o = 25\ \text{k}\Omega$.

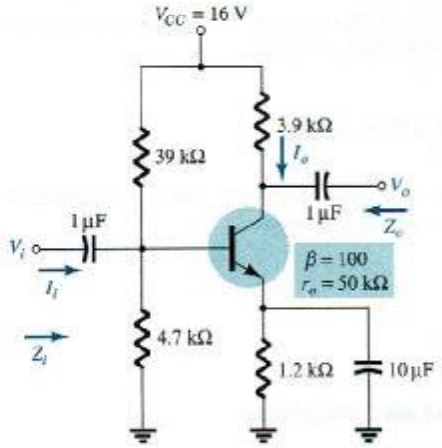


FIG. 5.153
Problem 12.

13. Determine V_{CC} for the network of Fig. 5.154 if $A_v = -160$ and $r_o = 100\ \text{k}\Omega$.

14. For the network of Fig. 5.155:
    a. Determine r_e.
    b. Calculate V_B and V_C.
    c. Determine Z_i and $A_v = V_o/V_i$.

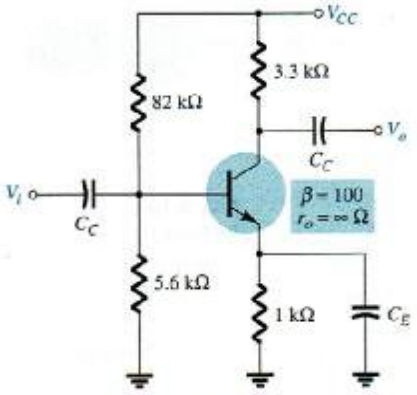


FIG. 5.154
Problem 13.

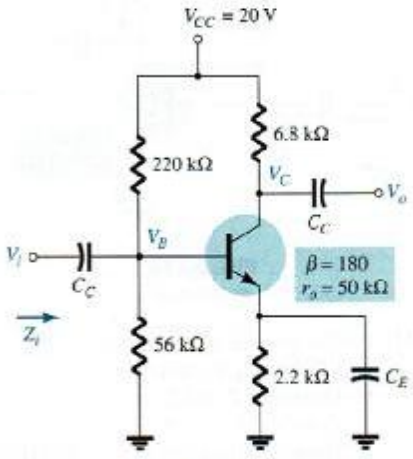


FIG. 5.155
Problem 14.

5.7 CE Emitter-Bias Configuration

15. For the network of Fig. 5.156:
    a. Determine r_e.
    b. Find Z_i and Z_o.
    c. Calculate A_v.
    d. Repeat parts (b) and (c) with $r_o = 20\ \text{k}\Omega$.

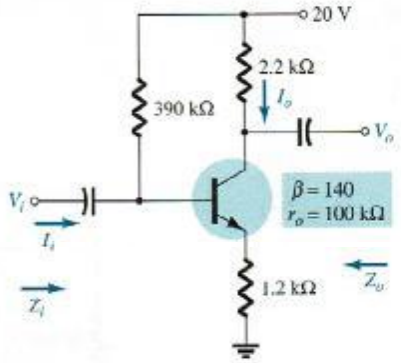


FIG. 5.156
Problems 15 and 17.

16. For the network of Fig. 5.157, determine R_E and R_B if $A_v = -10$ and $r_e = 3.8\ \Omega$. Assume that $Z_b = \beta R_E$.

17. Repeat Problem 15 with R_E bypassed. Compare results.

***18.** For the network of Fig. 5.158:
- **a.** Determine r_e.
- **b.** Find Z_i and A_v.

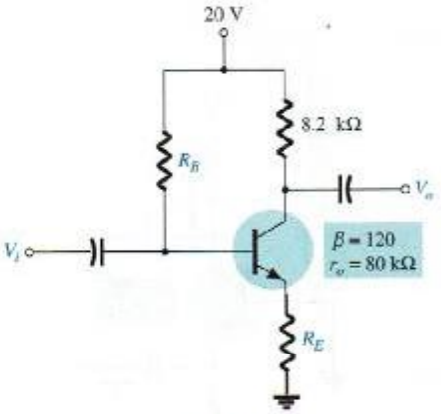


FIG. 5.157
Problem 16.

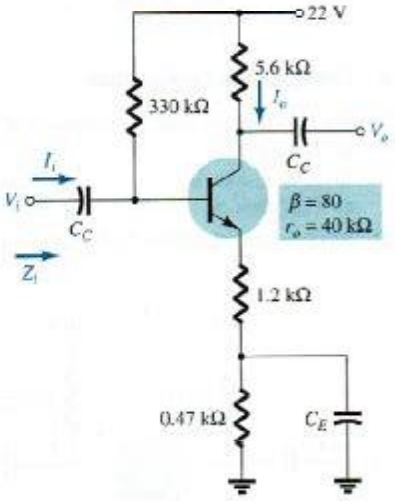


FIG. 5.158
Problem 18.

5.8 Emitter-Follower Configuration

19. For the network of Fig. 5.159:
- **a.** Determine r_e and βr_e.
- **b.** Find Z_i and Z_o.
- **c.** Calculate A_v.

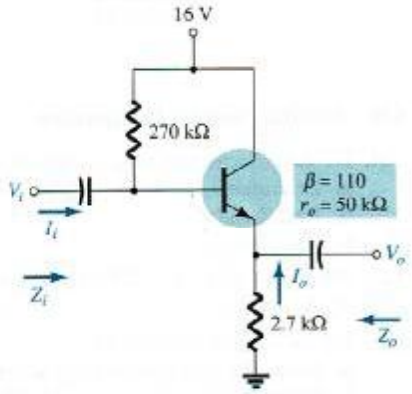


FIG. 5.159
Problem 19.

*20. For the network of Fig. 5.160:
   a. Determine Z_i and Z_o.
   b. Find A_v.
   c. Calculate V_o if $V_i = 1$ mV.

*21. For the network of Fig. 5.161:
   a. Calculate I_B and I_C.
   b. Determine r_e.
   c. Determine Z_i and Z_o.
   d. Find A_v.

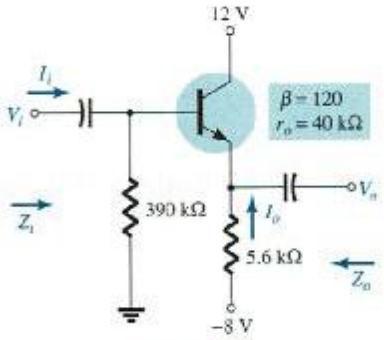


FIG. 5.160
Problem 20.

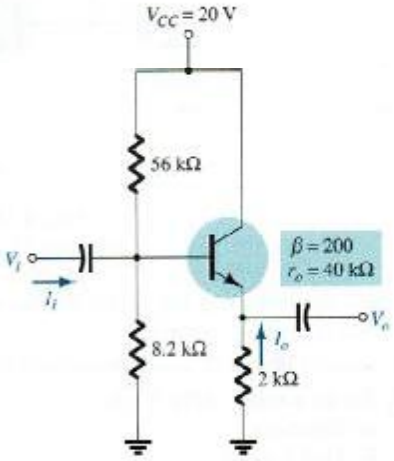


FIG. 5.161
Problem 21.

5.9 Common-Base Configuration

22. For the common-base configuration of Fig. 5.162:
   a. Determine r_e.
   b. Find Z_i and Z_o.
   c. Calculate A_v.

*23. For the network of Fig. 5.163, determine A_v.

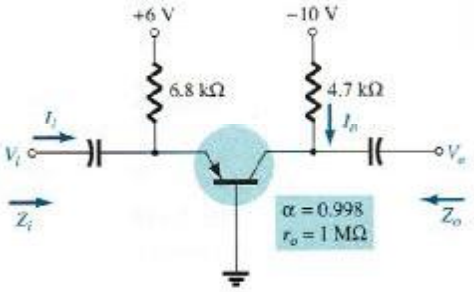


FIG. 5.162
Problem 22.

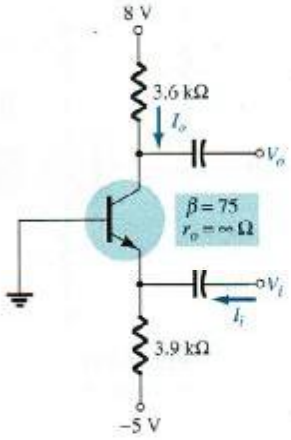


FIG. 5.163
Problem 23.

5.10 Collector Feedback Configuration

24. For the collector feedback configuration of Fig. 5.164:
   a. Determine r_e.
   b. Find Z_i and Z_o.
   c. Calculate A_v.

*25. Given $r_e = 10\ \Omega$, $\beta = 200$, $A_v = -160$, and $A_i = 19$ for the network of Fig. 5.165, determine R_C, R_F, and V_{CC}.

*26. For the network of Fig. 5.50:
   a. Derive the approximate equation for A_v.
   b. Derive the approximate equations for Z_i and Z_o.
   c. Given $R_C = 2.2$ kΩ, $R_f = 120$ kΩ, $R_E = 1.2$ kΩ, $\beta = 90$, and $V_{CC} = 10$ V, calculate the magnitudes of A_v, Z_i, and Z_o using the equations of parts (a) and (b).

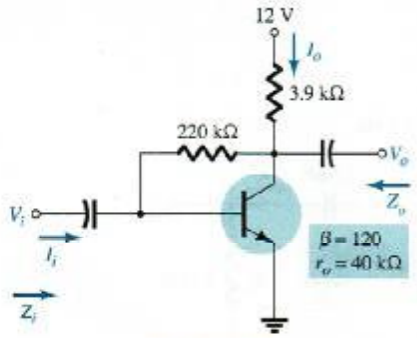


FIG. 5.164
Problem 24.

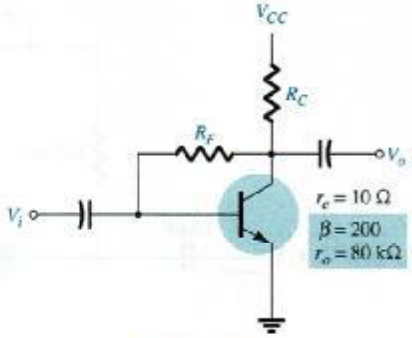


FIG. 5.165
Problem 25.

5.11 Collector DC Feedback Configuration

27. For the network of Fig. 5.166:
- **a.** Determine Z_i and Z_o.
- **b.** Find A_v.

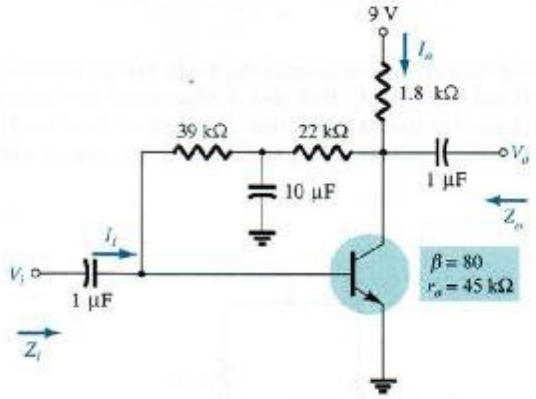


FIG. 5.166
Problem 27.

5.12 Determining the Current Gain

28. Determine the current gain for the common-emitter configuration of Fig. 5.150.

29. Determine the current gain for the common-emitter configuration of Fig. 5.152.

30. Determine the current gain for the voltage-divider network of Fig. 5.153.

31. Determine the current gain for the CE emitter-bias network of Fig. 5.156.

32. Determine the current gain for the emitter-follower configuration of Fig. 5.161.

33. Determine the current gain for the common-base configuration of Fig. 5.163.

34. Determine the current gain for the collector feedback configuration of Fig. 5.164.

35. Determine the current gain for the collector dc feedback configuration of Fig. 5.166.

5.13–5.15 Effect of R_i and R_s and Two-Port Systems Approach

***36.** For the fixed-bias configuration of Fig. 5.167:
- **a.** Determine A_{v_s}, Z_i, and Z_o.
- **b.** Sketch the two-port model of Fig. 5.63 with the parameters determined in part (a) in place.
- **c.** Calculate the gain A_{v_s}.
- **d.** Determine the current gain A_{i_s}.
- **e.** Determine A_{v_s}, A_{i_s}, Z_i, and Z_o using the r_e model and compare with the solutions above.

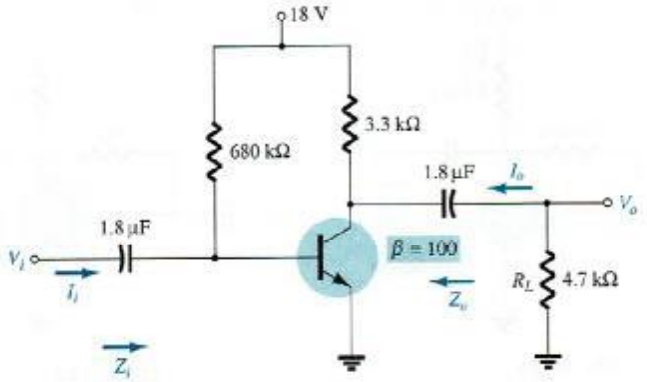


FIG. 5.167
Problems 36 and 37.

37. **a.** Determine the voltage gain A_{v_s} for the network of Fig. 5.167 for $R_L = 4.7$, 2.2, and 0.5 kΩ. What is the effect of decreasing levels of R_L on the voltage gain?
b. How will Z_i, Z_o, and $A_{v_{NL}}$ change with decreasing values of R_L?

***38.** For the network of Fig. 5.168:
a. Determine $A_{v_{NL}}$, Z_i, and Z_o.
b. Sketch the two-port model of Fig. 5.63 with the parameters determined in part (a) in place.
c. Determine A_v.
d. Determine A_{v_s}.
e. Determine A_{v_s} using the r_e model and compare the results to that obtained in part (d).
f. Change R_s to 1 kΩ and determine A_v. How does A_v change with the level of R_s?
g. Change R_s to 1 kΩ and determine A_{v_s}. How does A_{v_s} change with the level of R_s?
h. Change R_s to 1 kΩ and determine $A_{v_{NL}}$, Z_i, and Z_o. How do they change with change in R_s?

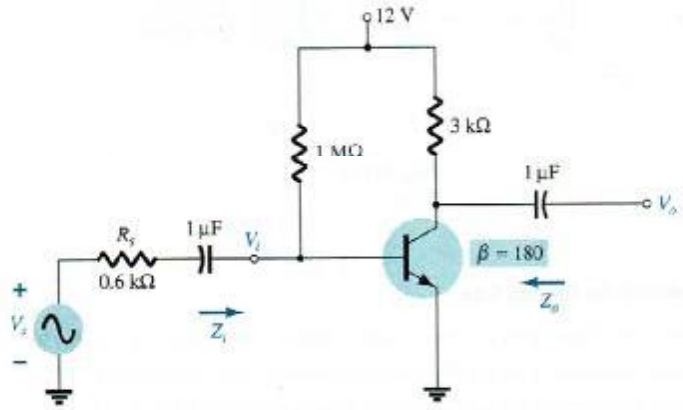


FIG. 5.168
Problem 38.

***39.** For the network of Fig. 5.169:
a. Determine $A_{v_{NL}}$, Z_i, and Z_o.
b. Sketch the two-port model of Fig. 5.63 with the parameters determined in part (a) in place.
c. Determine A_{v_s} and A_{i_s}.
d. Calculate A_{i_s}.
e. Change R_L to 5.6 kΩ and calculate A_{v_s}. What is the effect of increasing levels of R_L on the gain?
f. Change R_s to 0.5 kΩ (with R_L at 2.7 kΩ) and comment on the effect of reducing R_s on A_{v_s}.
g. Change R_L to 5.6 kΩ and R_s to 0.5 kΩ and determine the new levels of Z_i and Z_o. How are the impedance parameters affected by changing levels of R_L and R_s?

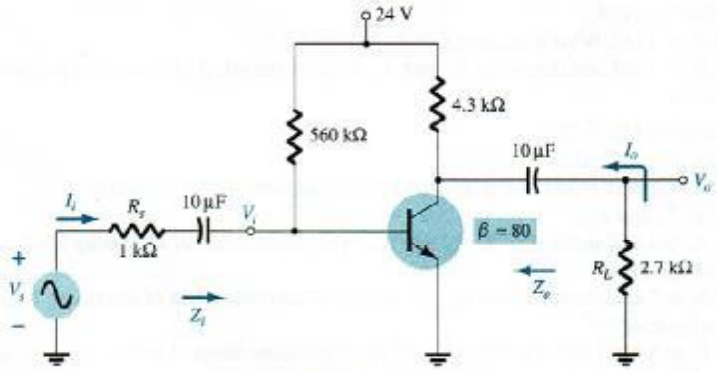


FIG. 5.169
Problem 39.

40. For the voltage-divider configuration of Fig. 5.170:
- **a.** Determine $A_{v_{NL}}$, Z_i, and Z_o.
- **b.** Sketch the two-port model of Fig. 5.63 with the parameters determined in part (a) in place.
- **c.** Calculate the gain A_{v_L}.
- **d.** Determine the current gain A_{i_L}.
- **e.** Determine A_{v_L}, A_{i_L}, and Z_o using the r_e model and compare solutions.

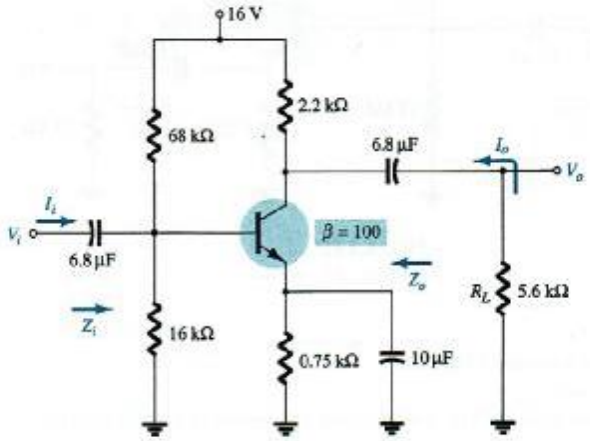


FIG. 5.170
Problem 40.

41. **a.** Determine the voltage gain A_{v_L} for the network of Fig. 5.170 with $R_L = 4.7, 2.2$, and $0.5\ \text{k}\Omega$. What is the effect of decreasing levels of R_L on the voltage gain?
- **b.** How will Z_i, Z_o, and $A_{v_{NL}}$ change with decreasing levels of R_L?

42. For the emitter-stabilized network of Fig. 5.171:
- **a.** Determine $A_{v_{NL}}$, Z_i, and Z_o.
- **b.** Sketch the two-port model of Fig. 5.63 with the values determined in part (a).

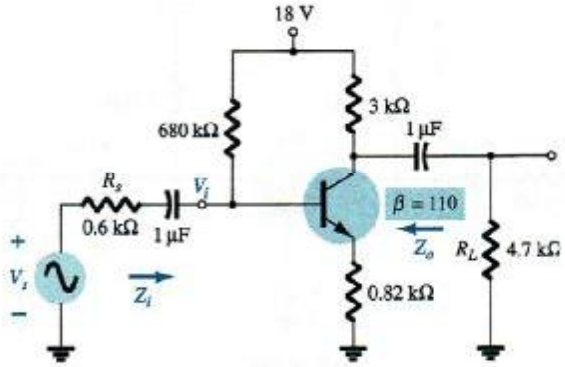


FIG. 5.171
Problem 42.

c. Determine A_{v_s} and A_{v_s}.
d. Change R_s to 1 kΩ. What is the effect on A_{v_s}, Z_i, and Z_o?
e. Change R_s to 1 kΩ and determine A_{v_s} and A_{v_s}. What is the effect of increasing levels of R_s on A_{v_s} and A_{v_s}?

*43. For the network of Fig. 5.172:
a. Determine $A_{v_{NL}}$, Z_i, and Z_o.
b. Sketch the two-port model of Fig. 5.63 with the values determined in part (a).
c. Determine A_{v_s} and A_{v_s}.
d. Change R_s to 1 kΩ and determine A_{v_s} and A_{v_s}. What is the effect of increasing levels of R_s on the voltage gains?
e. Change R_s to 1 kΩ and determine $A_{v_{NL}}$, Z_i, and Z_o. What is the effect of increasing levels of R_s on the parameters?
f. Change R_L to 5.6 kΩ and determine A_{v_s} and A_{v_s}. What is the effect of increasing levels of R_L on the voltage gains? Maintain R_s at its original level of 0.6 kΩ.

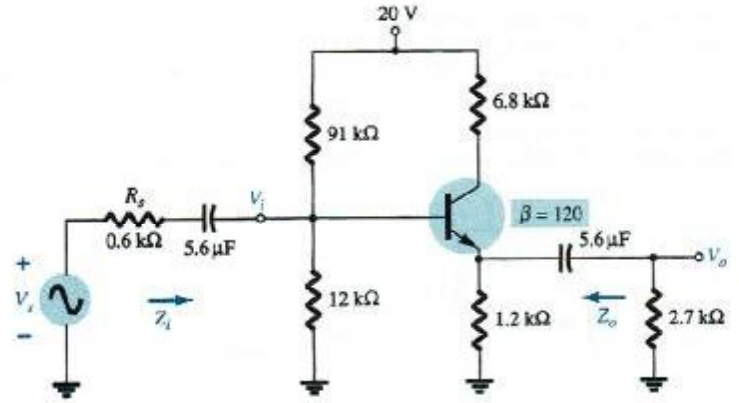


FIG. 5.172
Problem 43.

*44. For the common-base network of Fig. 5.173:
a. Determine Z_i, Z_o, and $A_{v_{NL}}$.
b. Sketch the two-port model of Fig. 5.63 with the parameters of part (a) in place.
c. Determine A_{v_s} and A_{v_s}.
d. Determine A_{v_s} and A_{v_s} using the r_e model and compare with the results of part (c).
e. Change R_s to 0.5 kΩ and R_L to 2.2 kΩ and calculate A_{v_s} and A_{v_s}. What is the effect of changing levels of R_s and R_L on the voltage gains?
f. Determine Z_o if R_s changed to 0.5 kΩ with all other parameters as appearing in Fig. 5.173. How is Z_o affected by changing levels of R_s?
g. Determine Z_i if R_L is reduced to 2.2 kΩ. What is the effect of changing levels of R_L on the input impedance?

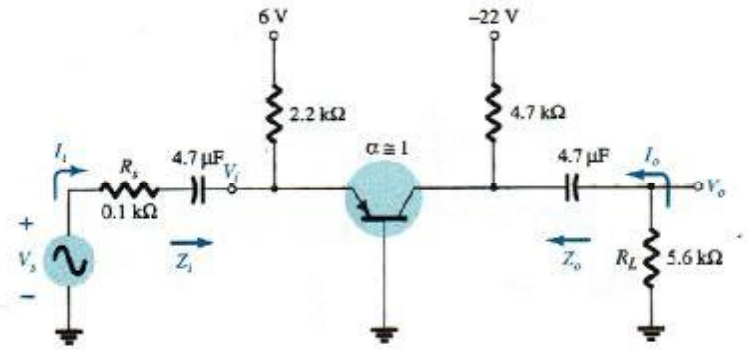


FIG. 5.173
Problem 44.

5.16 Cascaded Systems

*45. For the cascaded system of Fig. 5.174 with two identical stages, determine:
   a. The loaded voltage gain of each stage.
   b. The total gain of the system, A_v and A_{v_s}.
   c. The loaded current gain of each stage.
   d. The total current gain of the system.
   e. How Z_i is affected by the second stage and R_L.
   f. How Z_o is affected by the first stage and R_s.
   g. The phase relationship between V_o and V_i.

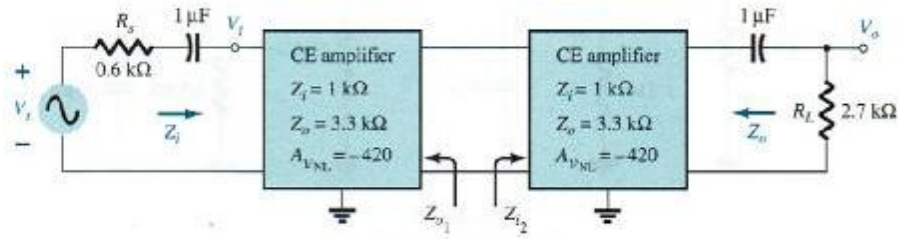


FIG. 5.174
Problem 45.

*46. For the cascaded system of Fig. 5.175, determine:
   a. The loaded voltage gain of each stage.
   b. The total gain of the system, A_v and A_{v_s}.
   c. The loaded current gain of each stage.
   d. The total current gain of the system.
   e. How Z_i is affected by the second stage and R_L.
   f. How Z_o is affected by the first stage and R_s.
   g. The phase relationship between V_o and V_i.

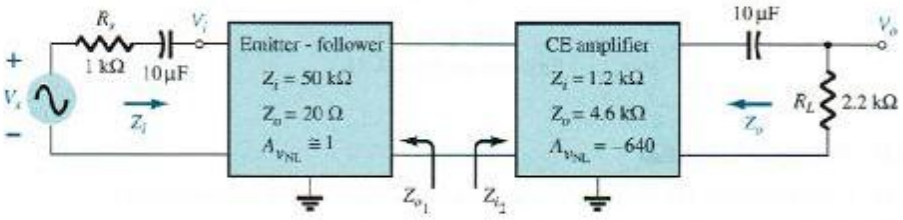


FIG. 5.175
Problem 46.

47. For the BJT cascade amplifier of Fig. 5.176, calculate the dc bias voltages and collector current for each stage.

48. Calculate the voltage gain of each stage and the overall ac voltage gain for the BJT cascade amplifier circuit of Fig. 5.176.

49. In the cascode amplifier circuit of Fig. 5.177, calculate the dc bias voltages V_{B_1}, V_{B_2}, and V_{C_2}.

*50. For the cascode amplifier circuit of Fig. 5.177, calculate the voltage gain A_v and output voltage V_o.

51. Calculate the ac voltage across a 10-kΩ load connected at the output of the circuit in Fig. 5.177.

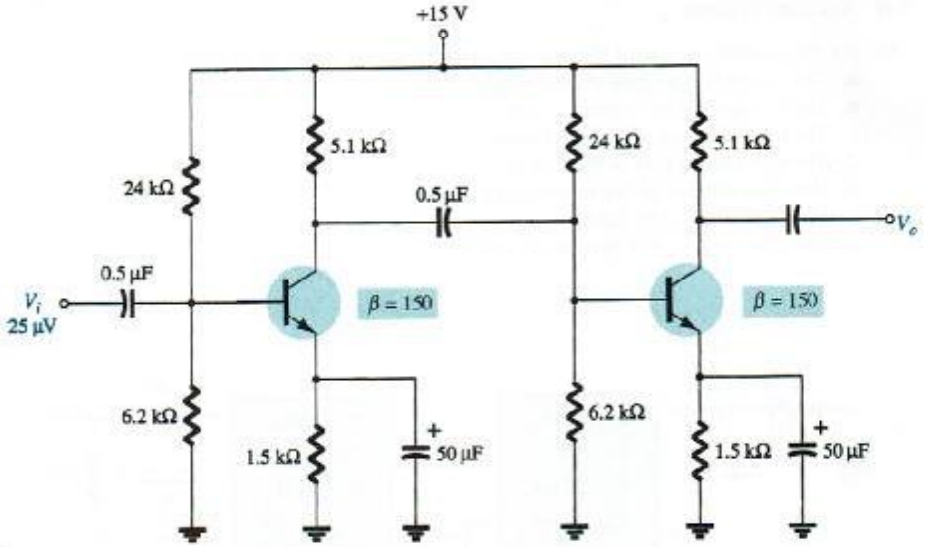


FIG. 5.176
Problems 47 and 48.

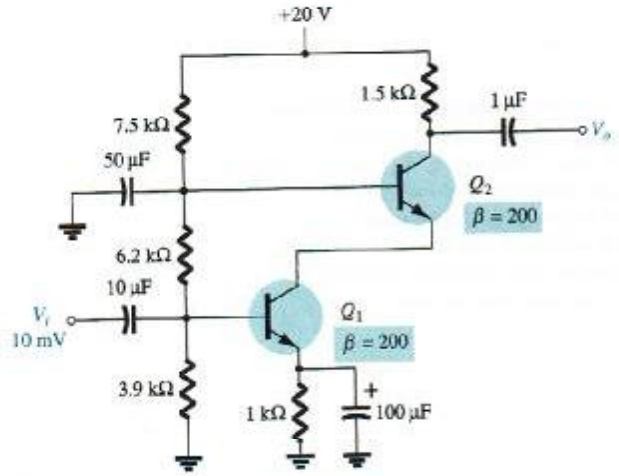


FIG. 5.177
Problems 49 through 51.

5.17 Darlington Connection

52. For the circuit of Fig. 5.178, calculate the dc bias voltage V_{E_1} and emitter current I_{E_1}.

*53. For the circuit of Fig. 5.178, calculate the amplifier voltage gain.

54. Repeat Problem 53 if a resistor $R_C = 200\ \text{k}\Omega$ is added along with a bypass capacitor C_E. The output is now off the collector of the transistors.

5.18 Feedback Pair

55. For the feedback pair circuit of Fig. 5.179, calculate the dc bias values of V_{B_1}, V_{C_1}, and I_C.

*56. Calculate the output ac voltage for the circuit of Fig. 5.179.

5.19 The Hybrid Equivalent Model

57. Given $I_E(\text{dc}) = 1.2\ \text{mA}$, $\beta = 120$, and $r_o = 40\ \text{k}\Omega$, sketch the following:
   a. Common-emitter hybrid equivalent model.
   b. Common-emitter r_e equivalent model.
   c. Common-base hybrid equivalent model.
   d. Common-base r_e equivalent model.

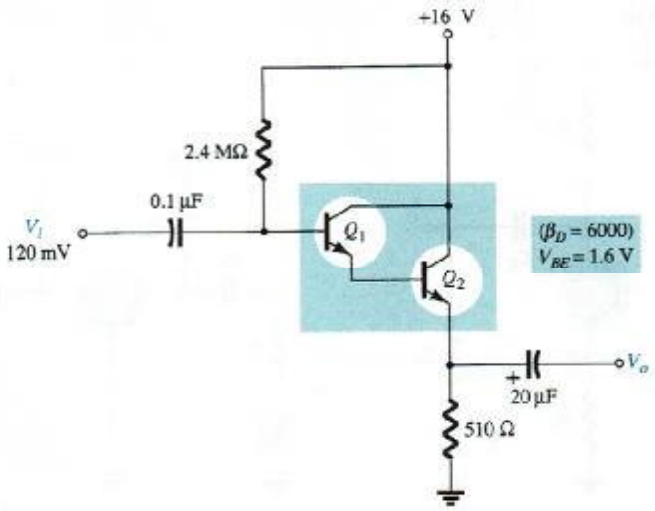


FIG. 5.178
Problems 52 and 53.

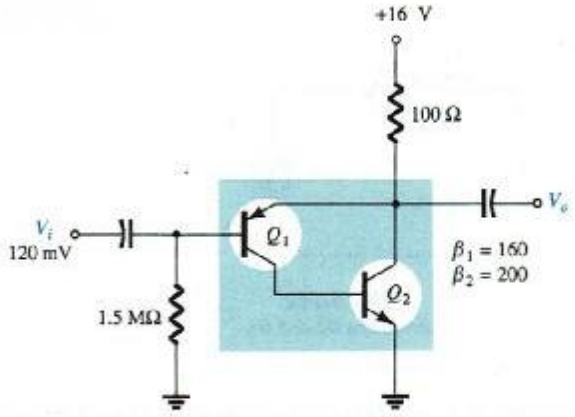


FIG. 5.179
Problems 55 and 56.

58. Given $h_{ie} = 2.4\ \text{k}\Omega$, $h_{fe} = 100$, $h_{re} = 4 \times 10^{-4}$, and $h_{oe} = 25\ \mu\text{S}$, sketch the following:
- **a.** Common-emitter hybrid equivalent model.
- **b.** Common-emitter r_e equivalent model.
- **c.** Common-base hybrid equivalent model.
- **d.** Common-base r_e equivalent model.

59. Redraw the common-emitter network of Fig. 5.3 for the ac response with the approximate hybrid equivalent model substituted between the appropriate terminals.

60. Redraw the network of Fig. 5.180 for the ac response with the r_e model inserted between the appropriate terminals. Include r_o.

61. Redraw the network of Fig. 5.181 for the ac response with the r_e model inserted between the appropriate terminals. Include r_o.

62. Given the typical values of $h_{ie} = 1\ \text{k}\Omega$, $h_{re} = 2 \times 10^{-4}$, and $A_v = -160$ for the input configuration of Fig. 5.182:
- **a.** Determine V_o in terms of V_i.
- **b.** Calculate I_b in terms of V_i.
- **c.** Calculate I_b if $h_{re}V_o$ is ignored.
- **d.** Determine the percentage difference in I_b using the following equation:

$$\%\ \text{difference in } I_b = \frac{I_b(\text{without } h_{re}) - I_b(\text{with } h_{re})}{I_b(\text{without } h_{re})} \times 100\%$$

- **e.** Is it a valid approach to ignore the effects of $h_{re}V_o$ for the typical values employed in this example?

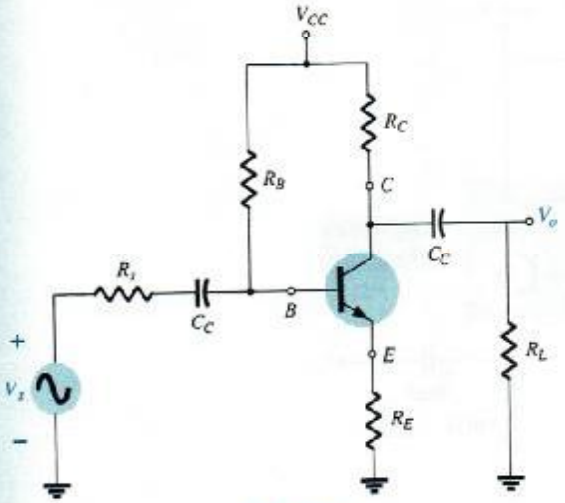


FIG. 5.180
Problem 60.

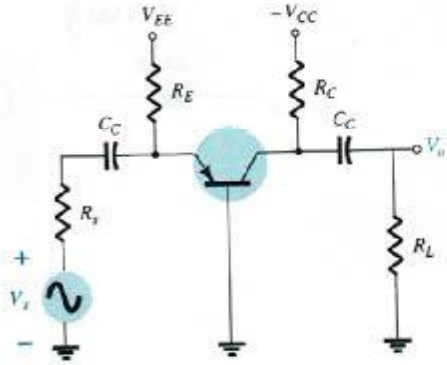


FIG. 5.181
Problem 61.

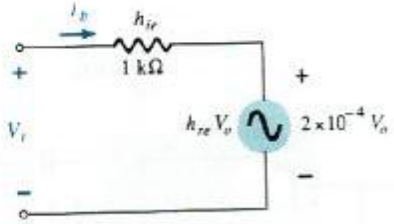


FIG. 5.182
Problems 62 and 64.

63. Given the typical values of $R_L = 2.2\ \text{k}\Omega$ and $h_{oe} = 20\ \mu\text{S}$, is it a good approximation to ignore the effects of $1/h_{oe}$ on the total load impedance? What is the percentage difference in total loading on the transistor using the following equation?

$$\%\ \text{difference in total load} = \frac{R_L - R_L \| (1/h_{oe})}{R_L} \times 100\%$$

64. Repeat Problem 62 using the average values of the parameters of Fig. 5.92 with $A_v = -180$.

65. Repeat Problem 63 for $R_L = 3.3\ \text{k}\Omega$ and the average value of h_{oe} in Fig. 5.92.

5.20 Approximate Hybrid Equivalent Circuit

66. **a.** Given $\beta = 120$, $r_e = 4.5\ \Omega$, and $r_o = 40\ \text{k}\Omega$, sketch the approximate hybrid equivalent circuit.

b. Given $h_{ie} = 1\ \text{k}\Omega$, $h_{re} = 2 \times 10^{-4}$, $h_{fe} = 90$, and $h_{oe} = 20\ \mu\text{S}$, sketch the r_e model.

67. For the network of Problem 9:

a. Determine r_e.

b. Find h_{fe} and h_{ie}.

c. Find Z_i and Z_o using the hybrid parameters.

d. Calculate A_v and A_i using the hybrid parameters.

e. Determine Z_i and Z_o if $h_{oe} = 50\ \mu\text{S}$.

f. Determine A_v and A_i if $h_{oe} = 50\ \mu\text{S}$.

g. Compare the solutions above with those of Problem 9. (Note: The solutions are available in Appendix E if Problem 9 was not performed.)

68. For the network of Fig. 5.183.

a. Determine Z_i and Z_o.

b. Calculate A_v and A_i.

c. Determine r_e and compare βr_e to h_{ie}.

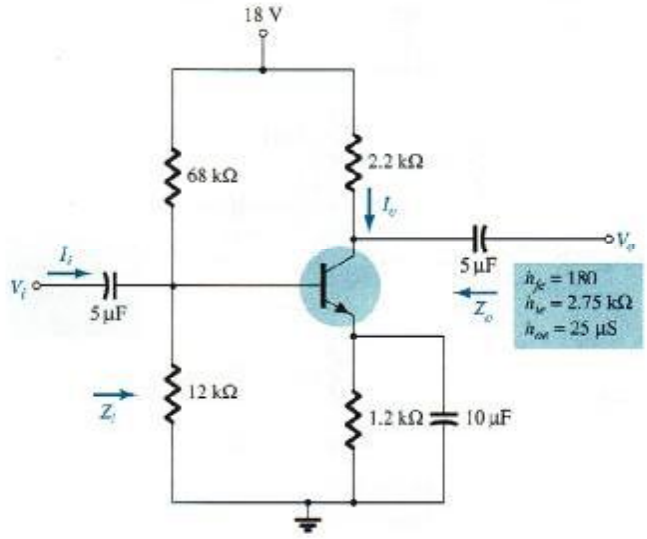


FIG. 5.183
Problem 68.

*69. For the common-base network of Fig. 5.184:
   a. Determine Z_i and Z_o.
   b. Calculate A_v and A_i.
   c. Determine α, β, r_e, and r_o.

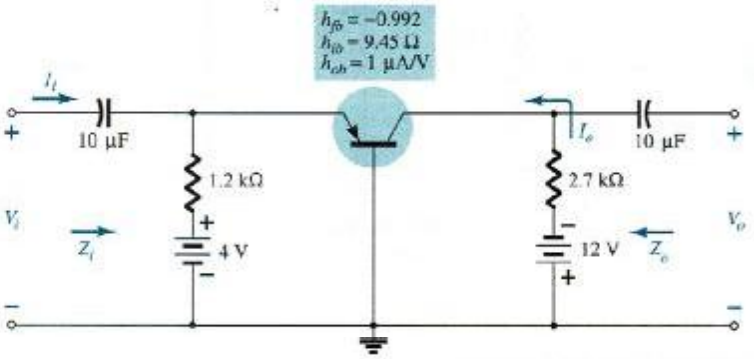


FIG. 5.184
Problem 69.

5.21 Complete Hybrid Equivalent Model

*70. Repeat parts (a) and (b) of Problem 68 with $h_{re} = 2 \times 10^{-4}$ and compare results.

*71. For the network of Fig. 5.185, determine:
   a. Z_i.
   b. A_v.
   c. $A_i = I_o/I_i$.
   d. Z_o.

*72. For the common-base amplifier of Fig. 5.186, determine:
   a. Z_i.
   b. A_i.
   c. A_v.
   d. Z_o.

5.22 Hybrid π Model

73. a. Sketch the Giacoletto (hybrid π) model for a common-emitter transistor if $r_b = 4\ \Omega$, $C_\pi = 5$ pF, $C_u = 1.5$ pF, $h_{oe} = 18\ \mu$S, $\beta = 120$, and $r_e = 14$.
   b. If the applied load is 1.2 kΩ and the source resistance is 250 Ω, draw the approximate hybrid π model for the low- and mid-frequency range.

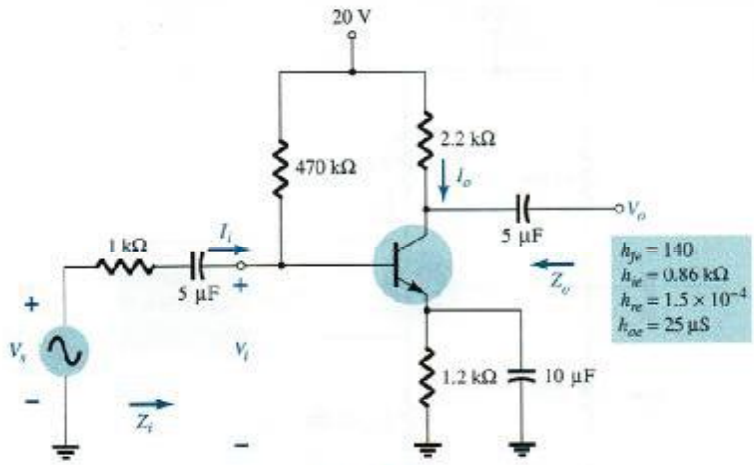


FIG. 5.185
Problem 71.

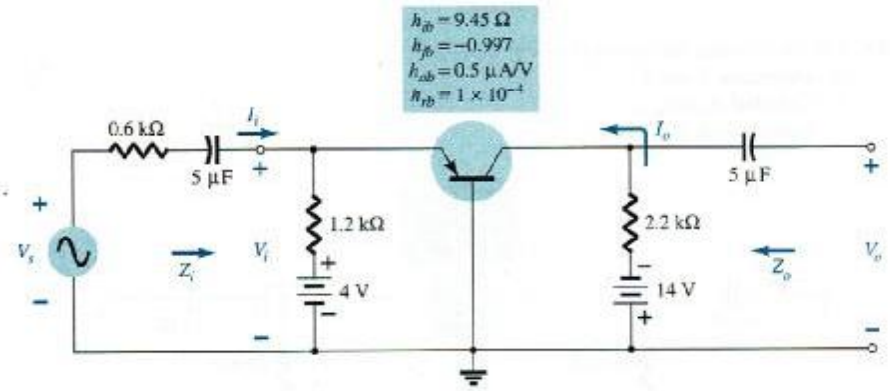


FIG. 5.186
Problem 72.

5.23 Variations of Transistor Parameters

For Problems 74 through 80, use Figs. 5.124 through 5.126.

74. **a.** Using Fig. 5.124, determine the magnitude of the percentage change in h_{fe} for an I_C change from 0.2 mA to 1 mA using the equation

$$\%\ \text{change} = \left| \frac{h_{fe}(0.2\ \text{mA}) - h_{fe}(1\ \text{mA})}{h_{fe}(0.2\ \text{mA})} \right| \times 100\%$$

b. Repeat part (a) for an I_C change from 1 mA to 5 mA.

75. Repeat Problem 74 for h_{ie} (same changes in I_C).

76. **a.** If $h_{oe} = 20\ \mu\text{S}$ at $I_C = 1$ mA on Fig. 5.124, what is the approximate value of h_{oe} at $I_C = 0.2$ mA?

b. Determine its resistive value at 0.2 mA and compare to a resistive load of 6.8 kΩ. Is it a good approximation to ignore the effects of $1/h_{oe}$ in this case?

77. **a.** If $h_{oe} = 20\ \mu\text{S}$ at $I_C = 1$ mA of Fig. 5.124, what is the approximate value of h_{oe} at $I_C = 10$ mA?

b. Determine its resistive value at 10 mA and compare to a resistive load of 6.8 kΩ. Is it a good approximation to ignore the effects of $1/h_{oe}$ in this case?

78. **a.** If $h_{re} = 2 \times 10^{-4}$ at $I_C = 1$ mA on Fig. 5.124, determine the approximate value of h_{re} at 0.1 mA.

b. For the value of h_{re} determined in part (a), can h_{re} be ignored as a good approximation if $A_v = 210$?

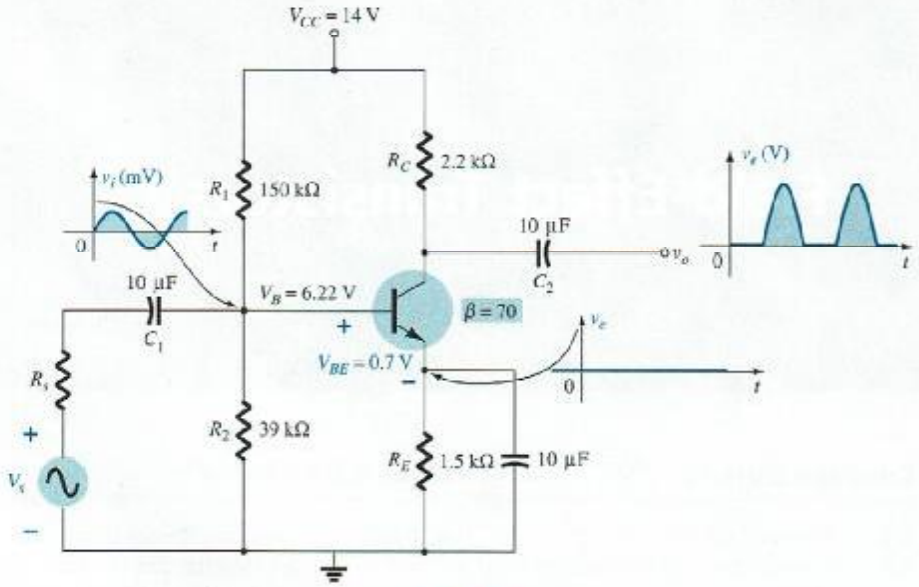


FIG. 5.187
Problem 81.

79. **a.** Based on a review of the characteristics of Fig. 5.124, which parameter changed the least for the full range of collector current?
b. Which parameter changed the most?
c. What are the maximum and minimum values of $1/h_{oe}$? Is the approximation $1/h_{oe} \| R_L \cong R_L$ more appropriate at high or low levels of collector current?
d. In which region of current spectrum is the approximation $h_{re}V_{ce} \cong 0$ the most appropriate?

80. **a.** Based on a review of the characteristics of Fig. 5.126, which parameter changed the most with increase in temperature?
b. Which changed the least?
c. What are the maximum and minimum values of h_{fe}? Is the change in magnitude significant? Was it expected?
d. How does r_e vary with increase in temperature? Simply calculate its level at three or four points and compare their magnitudes.
e. In which temperature range do the parameters change the least?

5.24 Troubleshooting

*81. Given the network of Fig. 5.187:
a. Is the network properly biased?
b. What problem in the network construction could cause V_B to be 6.22 V and obtain the given waveform of Fig. 5.187?

5.27 Computer Analysis

82. Using PSpice Windows, determine the voltage gain for the network of Fig. 5.25. Use Probe to display the input and output waveforms.

83. Using PSpice Windows, determine the voltage gain for the network of Fig. 5.32. Use Probe to display the input and output waveforms.

84. Using PSpice Windows, determine the voltage gain for the network of Fig. 5.45. Use Probe to display the input and output waveforms.

85. Using Multisim, determine the voltage gain for the network of Fig. 5.28.

86. Using Multisim, determine the voltage gain for the network of Fig. 5.40.

87. Using PSpice Windows, determine the level of V_o for $V_i = 1$ mV for the network of Fig. 5.71. For the capacitive elements assume a frequency of 1 kHz.

88. Repeat Problem 87 for the network of Fig. 5.72.

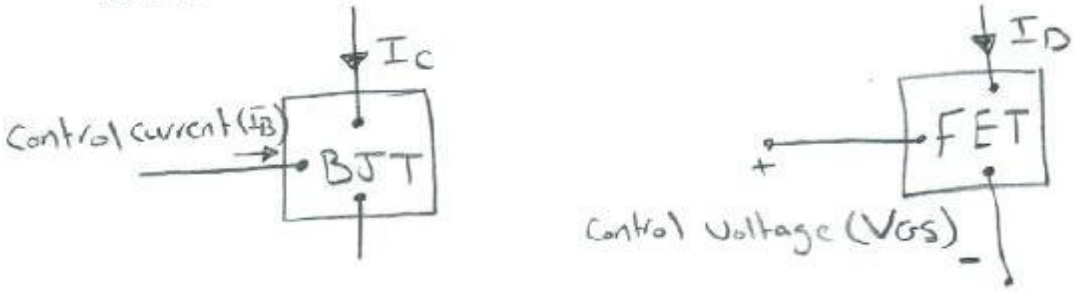
89. Repeat Problem 87 for the network of Fig. 5.79.

90. Repeat Problem 87 using Multisim.

91. Repeat Problem 87 using Multisim.

Field-Effect Transistors (FET):

The FET is a three terminal device used for a variety of applications, similar to the BJT transistor. The BJT and FET transistors have many similarities and differences but the primary difference between them is that **the BJT is a current-controlled device, whereas the FET transistor is a voltage controlled device** as shown below:



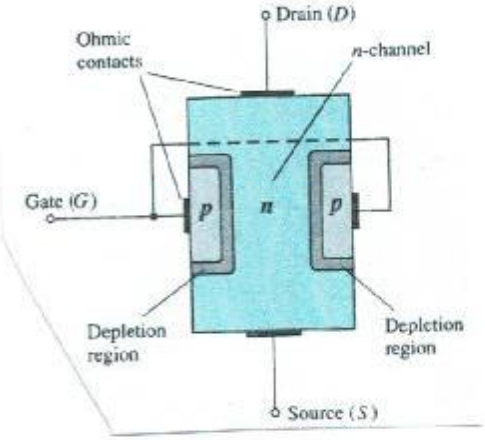
- For the BJT (pnp and npn).
- For the FET transistor there are:
  1. n-channel FET.
  2. p-channel FET.
- The FET transistor has very high input impedance, much higher than the input impedance of the BJT transistor.
- The ac voltage gain for BJT amplifiers are greater than for FETs.
- FETs are more temperature stable than BJTs and FETs are usually smaller than BJTs, making the FET transistor useful in integrated circuits (IC) chips.

In the following FET transistor study two types of FETs are introduced:

1. The Junction Field Effect transistor (JFET)
2. The Metal Oxide Semiconductor Field effect transistor (MOSFET) which also has two types:
   - The depletion type MOSFET.
   - Enhancement type MOSFET.

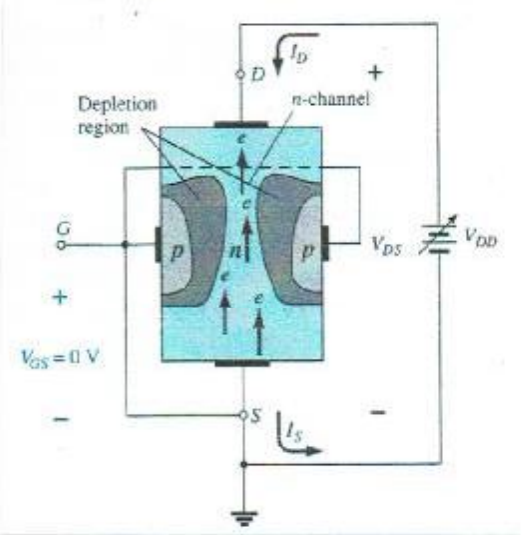
Construction and Characteristics of JFETs

The basic construction of the n-channel JFET is shown below:



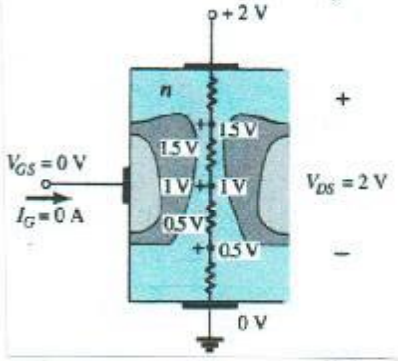
In the JFET there are two p-n junctions, so in the absence of any applied potentials the JFET has two p-n junctions under no-bias conditions. The result is a depletion region at each junction as is shown in the figure above.

If V_{GS} = 0V, V_{DS} = some positive value

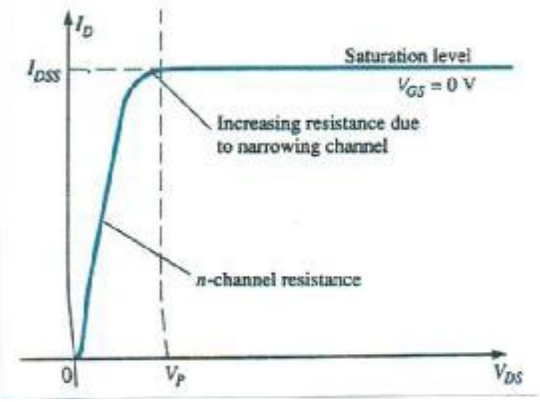


- If V_{GS} = 0V the depletion regions of the p-n junctions will be the same as the no bias condition.
- The instant V_{DD} (=V_{DS}) is applied then electrons are drawn to the drain and a current I_D will flow in the direction shown in the figure above.

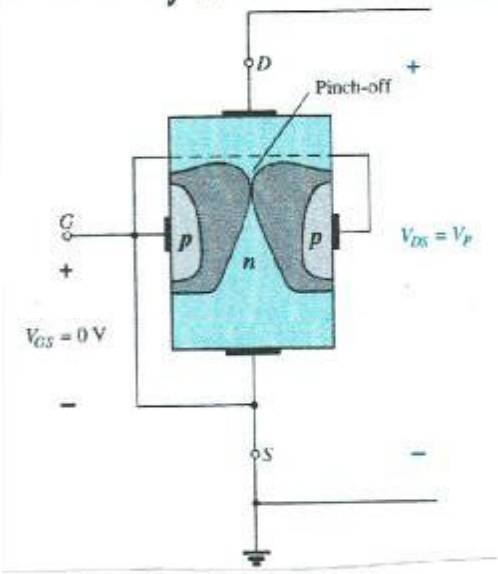
- Now as I_D flows, the depletion region will be wider near the top of both p-type materials. The reason for the change in width of the depletion region is shown below:



- The reason is that the upper region will be more reverse biased than the lower regions, therefore it will be wider.
- Also due to the reverse bias of both p-n junctions the current through the gate is zero (I_G = 0 A).
- As the voltage V_{DS} is increased the current I_D will increase as determined by ohm's law and the plot of I_D versus V_{DS} is shown below:



- If V_{DS} is increased further the two depletion regions will widen to a level where it appears that they would "touch" as shown in the following figure:



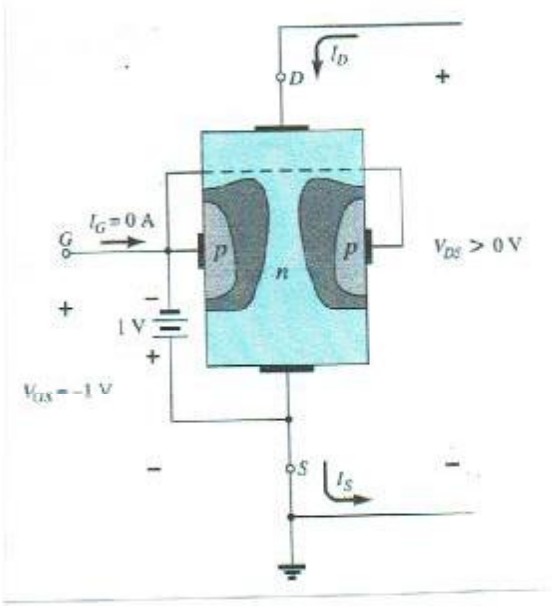
- The condition when the two depletion regions will touch is referred to as **pinch-off**, at this condition the level of V_{DS} is referred to as the **pinch-off voltage (V_P)**.
- At the pinch-off voltage **(V_P)** the current I_D will maintain a saturation level I_{DSS} and will not drop to zero.

  Note: if I_D drops to zero at V_P as the name refers to, it would remove the different voltage levels through the n-channel to establish the varying levels of reverse bias along the p-n junction. Therefore I_D will maintain a saturation level = I_{DSS} when V_{GS} =0V and $V_{DS} > V_P$.

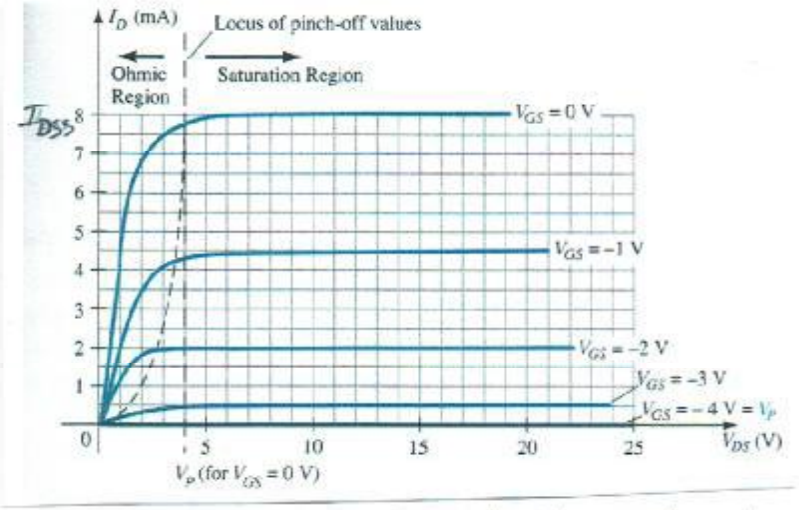
I_{DSS} drain to source current with a short circuit connection from gate-to-source.

- I_{DSS} is the maximum drain current for a JFET and is defined by the conditions V_{GS} = 0V and $V_{DS} > |V_P|$.

If V_{GS} < 0V

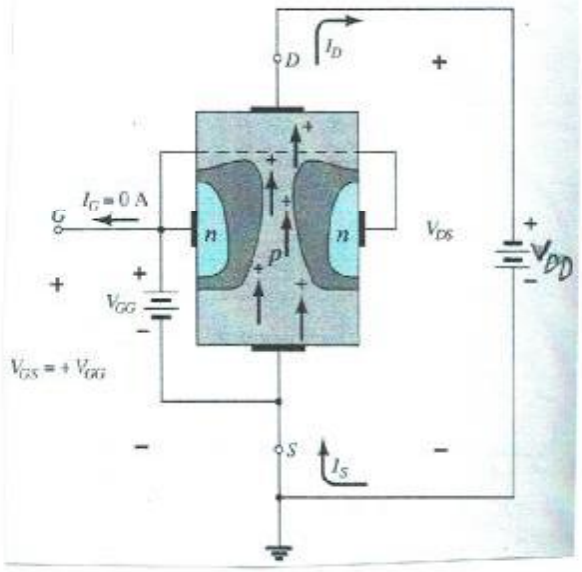


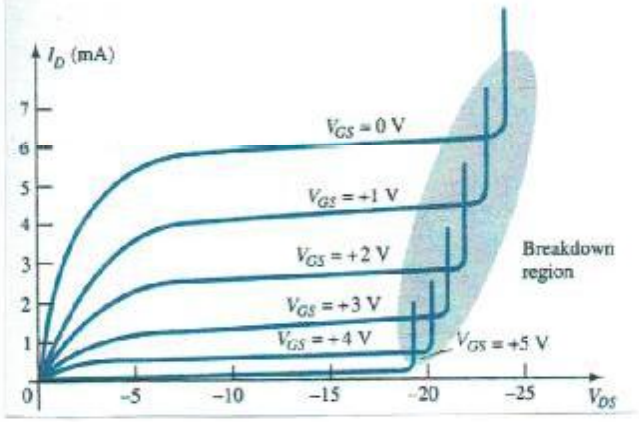
- The effect of applying negative-bias V_{GS} is to reach the saturation level at a lower level of V_{DS} as shown in the following figure:



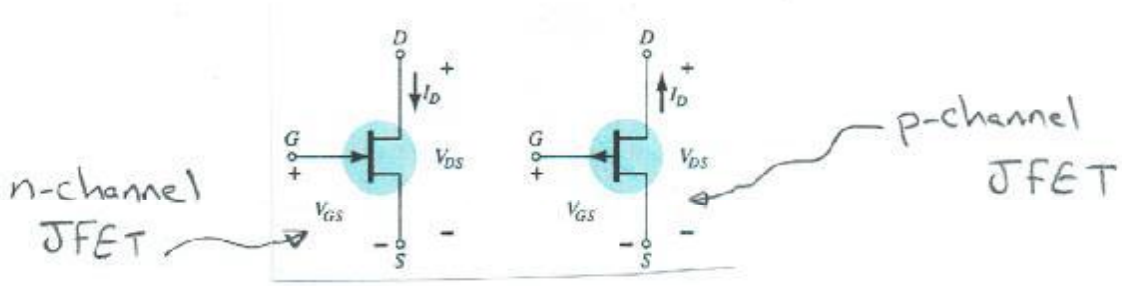
- The resulting saturation level of I_D has been reduced and will continue to decrease as V_{GS} is made more and more negative.
- Note also in the c/c's curve that the pinch-off voltage continues to drop in a parabolic manner as V_{GS} becomes more and more negative.
- I_D = 0mA at $V_{GS} = -|V_P|$ and the device is turned off.
- The level of V_{GS} that results in I_D = 0mA is defined by $V_{GS} = V_P$, with V_P being a negative voltage for n-channel JFETs and a positive voltage for p-channel JFETs.

p-channel JFETs:





JFET Symbol:



Summary:

- The maximum current is defined as I_{DSS} and occurs when V_{GS} = 0V and $V_{DS} \geq |V_P|$.
- For V_{GS} less than (more negative than) V_P, the drain current is 0A (I_D = 0A) .
- For all levels of V_{GS} between 0V and the pinch-off level, the current I_D will range between I_{DSS} and 0A.
- A similar list can be developed for p-channel JFETs.

Transfer Characteristics:

For the BJT transistor I_C and I_B are related by β :

$$I_C = \beta I_B$$

control variable

Constant

linear relationship

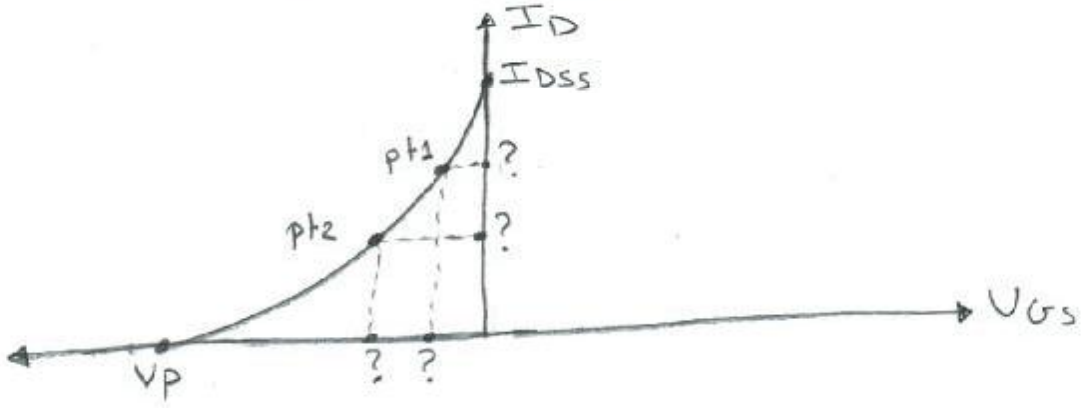
For the FET transistor I_D and V_{GS} are related by shockley's equation:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

Control variable

non-linear relationship

Constants



The above transfer curve (I_D versus V_{GS}) can be obtained directly from shockley's equation as in the following:

Substituting $V_{GS} = 0V$ gives:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$= I_{DSS}\left(1 - \frac{0}{V_P}\right)^2 = I_{DSS}$$

$$\boxed{I_D = I_{DSS}\big|_{V_{GS}=0V}}$$

Substituting $V_{GS} = V_P$ gives:

$$I_D = I_{DSS}\left(1 - \frac{V_P}{V_P}\right)^2$$

$$= I_{DSS}(1-1)^2 = 0A$$

$$\boxed{I_D = 0A\big|_{V_{GS}=V_P}}$$

From shockley's equation an equation for V_{GS} can be obtained:

$$V_{GS} = V_P\left(1 - \sqrt{\frac{I_D}{I_{DSS}}}\right)$$

To plot the transfer curve as simple as possible, four points are sufficient. So the previous two points of (I_D=0, V_{GS}=V_P) and (I_D=I_{DSS}, V_{GS}=0) are used and two others can be found as in the following:

- If $V_{GS} = \frac{1}{2} V_P$ ·

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = I_{DSS}\left(1 - \frac{V_P/2}{V_P}\right)^2$$

$$= I_{DSS}\left(1 - \frac{1}{2}\right)^2 = I_{DSS}\left(\frac{1}{2}\right)^2 = \frac{1}{4} I_{DSS}$$

$$\boxed{I_D = \frac{I_{DSS}}{4}} \quad V_{GS} = V_P/2$$

- If $I_D = \frac{I_{DSS}}{2}$

$$V_{GS} = V_P\left(1 - \sqrt{\frac{I_D}{I_{DSS}}}\right)$$

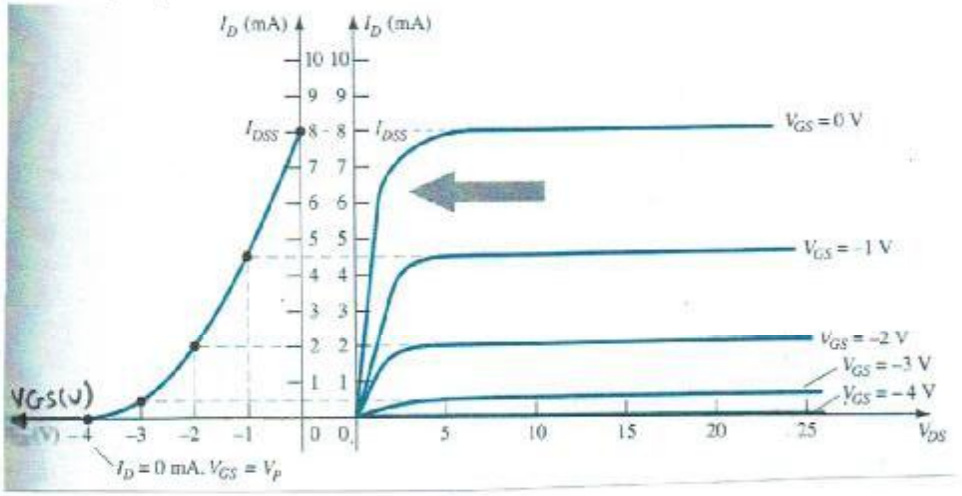
$$= V_P\left(1 - \sqrt{\frac{I_{DSS}/2}{I_{DSS}}}\right) = V_P\left(1 - \sqrt{0.5}\right) = V_P * 0.293$$

$$\boxed{I_D \cong 0.3\, V_P \quad | I_D = I_{DSS}/2}$$

In summary:

V_{GS}	I_D
0	I_{DSS}
$0.3V_P$	$I_{DSS}/2$
$0.5V_P$	$I_{DSS}/4$
V_P	0mA

Or the transfer curve can be obtained from the drain c/c's as shown in the following figure:



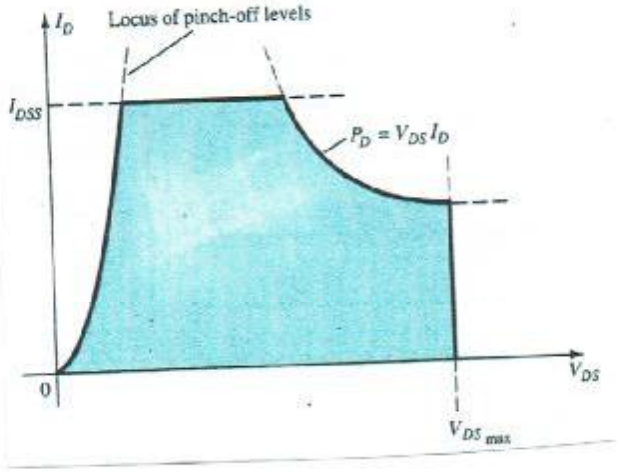
Example 6.1

Note:

For the p-channel JFETs shockley's equation can be applied, but **V_P and V_{GS}** will be **positive** and the **transfer curve** will be the **mirror image** of the one obtained for **n-channel** JFETs.

Example 6.2

Operating Region:



Important Relations:

JFET

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$I_D = I_S$

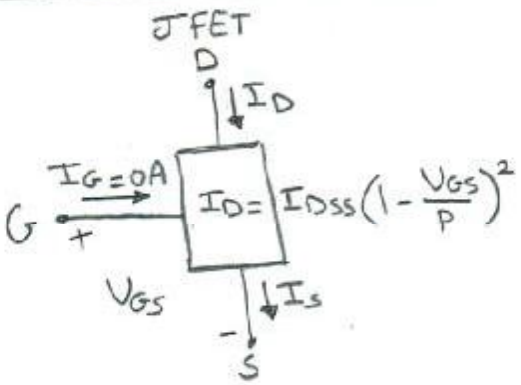
$I_G = 0\ A$

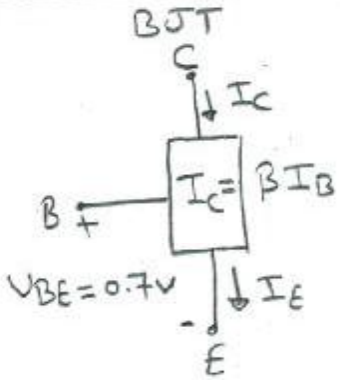
BJT

$I_C = \beta I_B$

$I_C \cong I_E$

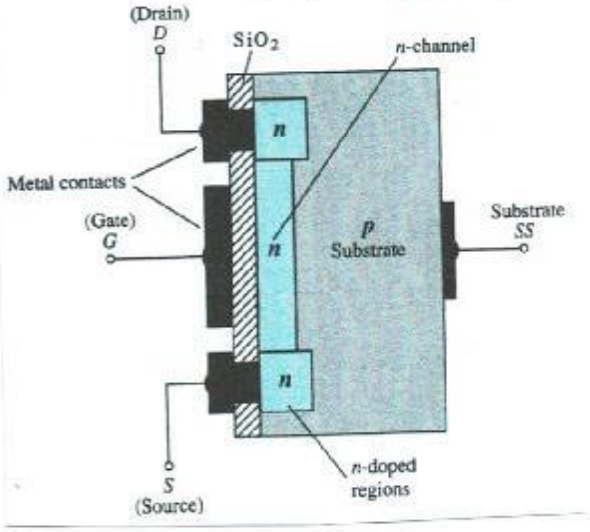
$V_{BE} \cong 0.7\ V$

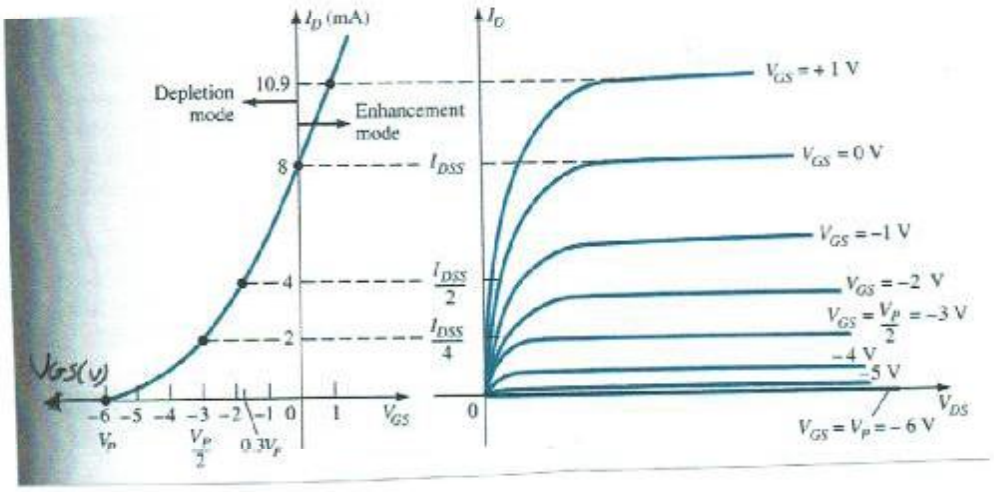




Depletion-Type MOSFET:

The MOSFET (Metal-Oxide-Semiconductor) has very desirable high input impedance due to the insulating layer Sio_2 ($I_G = 0$).



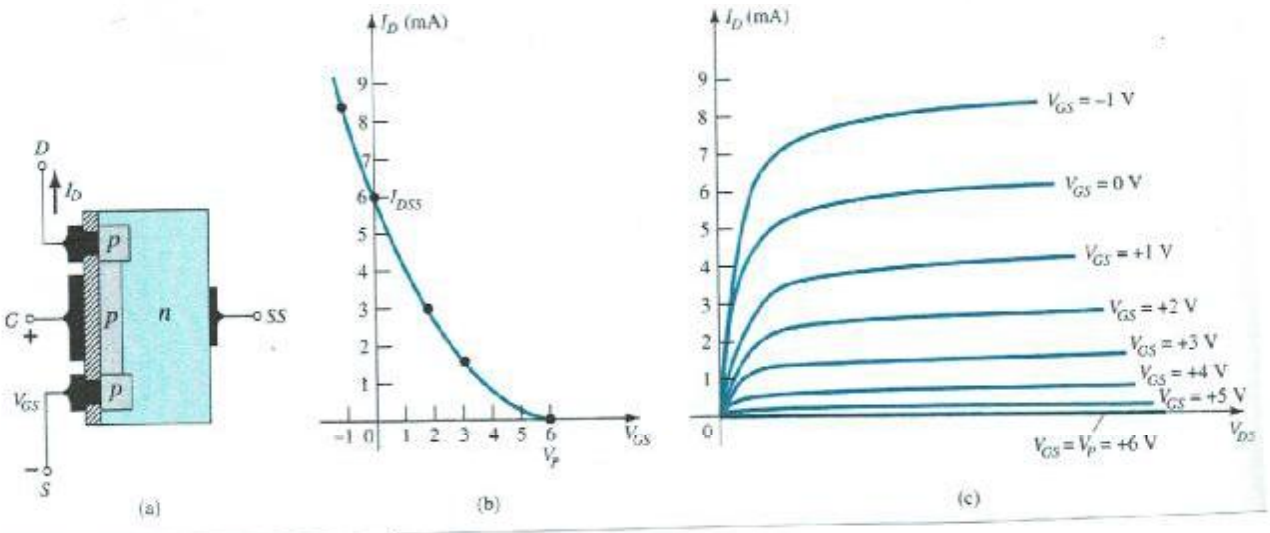


Note:

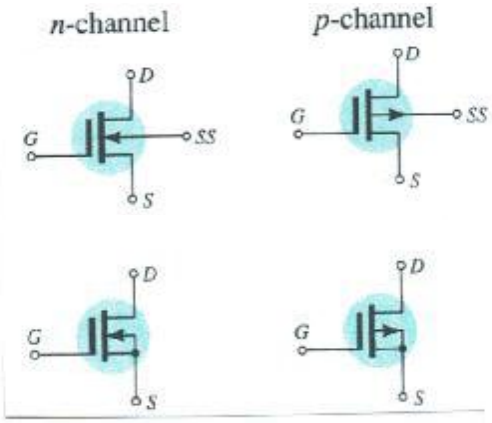
Shockley's equation continues to be applicable for the depletion-type MOSFET in both the depletion and enhancement regions. It is important to use the proper sign with V_{GS}, since negative for the depletion region and positive for the enhancement region.

Example 6.3

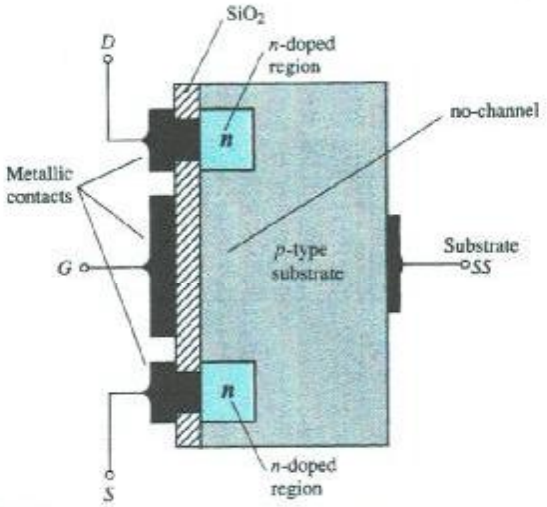
p-type Depletion Type MOSFET:



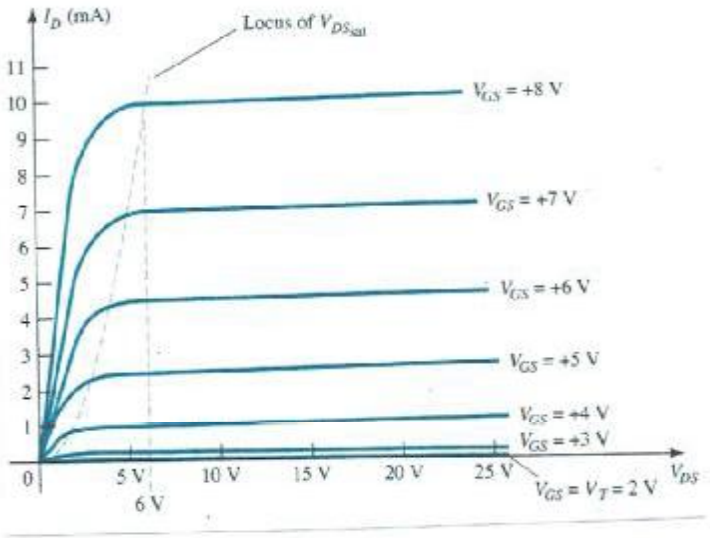
Depletion-Type MOSFET Symbol:



Enhancement-Type MOSFET:



- In the enhancement-type MOSFET the transfer curve is not defined by shockley's equation, and the drain current is now cut off until V_{GS} reaches a specific magnitude called threshold voltage (V_T).
- In n-channel depletion-type MOSFETs the current I_D is affected by a positive V_{GS}.



$V_{DSsat.} = V_{GS} - V_T$

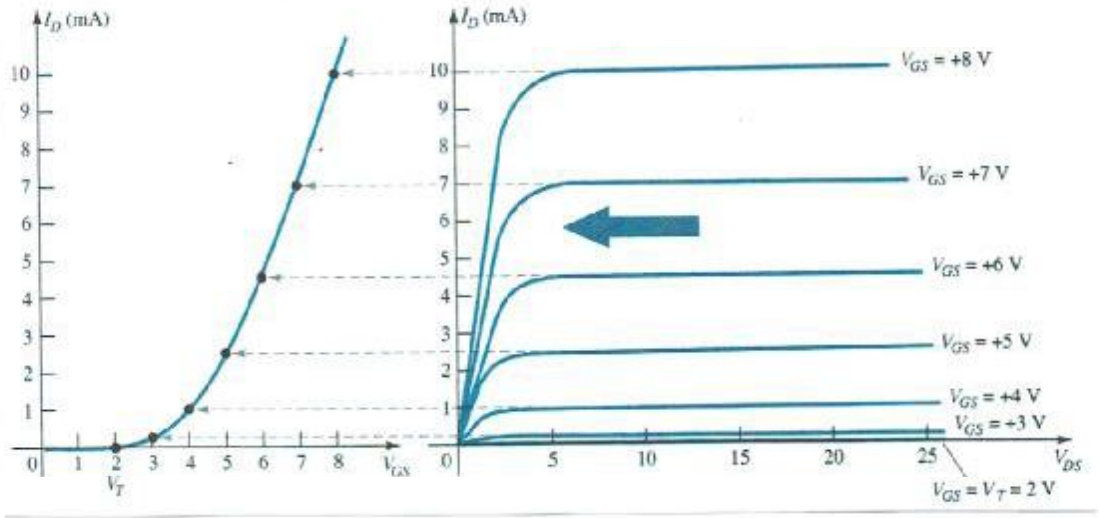
For $V_{GS} > V_T$ the drain current (I_D) is related to V_{GS} by the following equation:

$$I_D = K(V_{GS} - V_T)^2$$

K: constant

$$K = \frac{I_{D(on)}}{(V_{GS(on)} - V_T)^2}$$

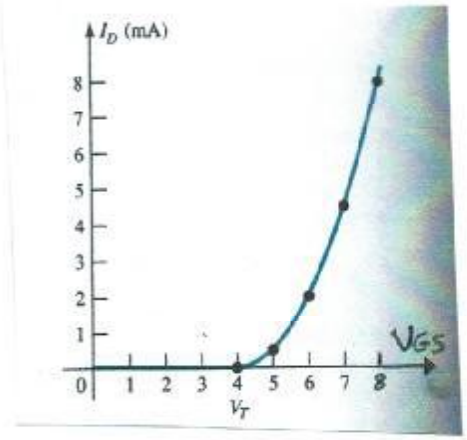
The transfer curve can be obtained from the drain c/c's ~~as in the following figure~~ by setting them side to side to describe the transfer process from one to the other as shown in the figure below:



$I_D = 0$ for $V_{GS} \leq V_T$.

The transfer curve can also be found if k and V_T are known by substituting value of V_{GS} and finding the value of I_D using the equation:

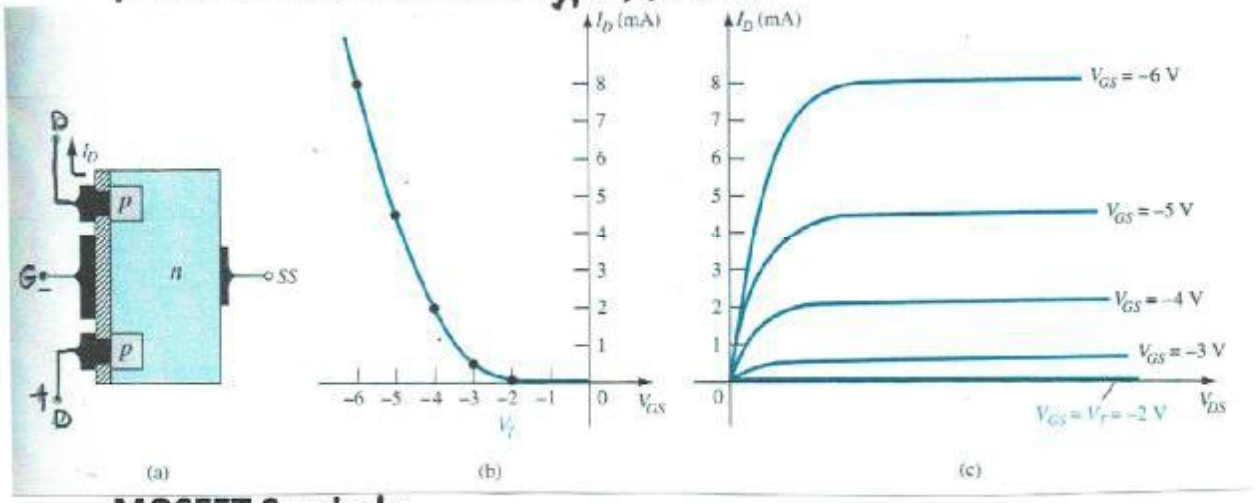
$$I_D = K(V_{GS} - V_T)^2$$



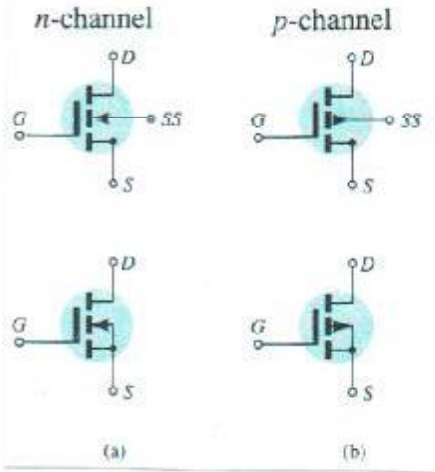
if $k = 0.5 * 10^{-3}$ A/V²

$V_T = 4$V

p-channel Enhancement-Type MOSFET:



MOSFET Symbols:



FET Biasing

The biasing levels of an FET transistor (I_D, V_{GS}) can be found either using direct mathematical approach or using graphical approach. In FET transistors the mathematical approach is complicated due to non-linear relationship between I_D and V_{GS} therefore the graphical approach will be used.

For all FET transistors the following is applied:

$$I_G = 0A$$

$$I_D = I_S$$

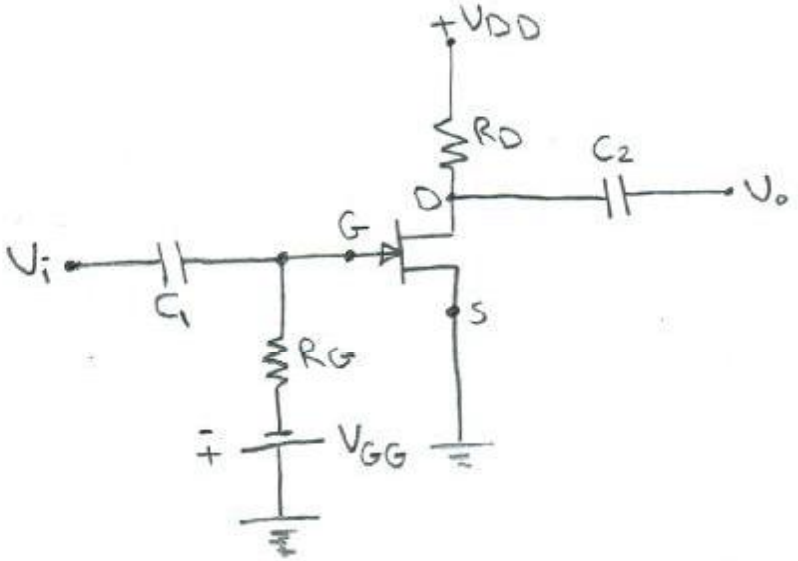
For JFETs and depletion-type MOSFETs, shockley's equation is applied to relate I_D and V_{GS}:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

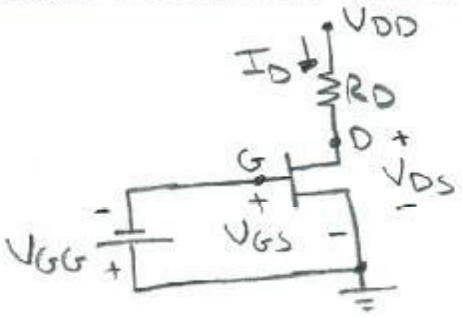
For enhancement-type MOSFETs, the following equation is applicable:

$$I_D = K(V_{GS} - V_T)^2$$

Fixed-Bias Configuration:



For dc analysis all the coupling capacitors are open circuits. The resulting network for dc analysis is shown in the figure below:



Since $I_G = 0A$

$$V_{R_G} = I_G R_G = (0A) R_G = 0V$$

$\therefore R_G$ is replaced by a short-circuit equivalent.

<u>The mathematical approach:</u>

Applying Kirchhoff's voltage law at the input loop (the gate-source loop) gives:

$$-V_{GG} - V_{GS} = 0$$

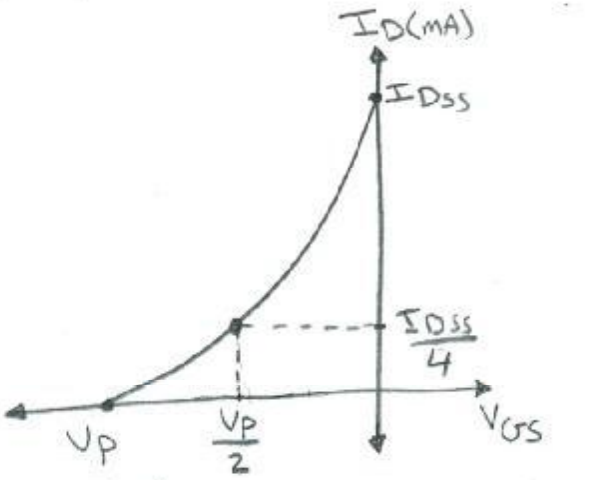
$$\boxed{V_{GS} = -V_{GG}}$$

Substituting the value of V_{GS} into shockley's equation to obtain the value of I_D.

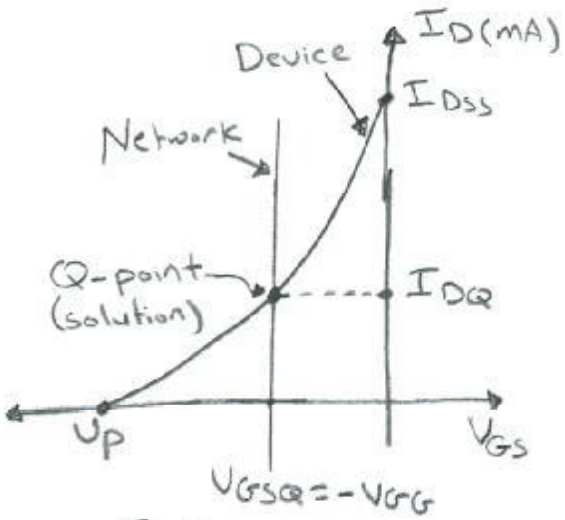
Using the graphical approach:

Using the table:

V_{GS}	I_D
0	I_{DSS}
$0.3V_P$	$I_{DSS}/2$
$0.5V_P$	$I_{DSS}/4$
V_P	0mA



plotting shockley's equation



Finding the solution for the fixed-bias configuration

From the previous figure the Q-point is found, which is the point where the two curves intersect.

V_{DS} can be found by applying Kirchhoff's voltage law as follows:

$$V_{DS} + I_D R_D - V_{DD} = 0$$

$$\boxed{V_{DS} = V_{DD} - I_D R_D}$$

$$\boxed{V_S = 0V}$$

$$V_{DS} = V_D - V_S \quad , \quad V_D = V_{DS} + V_S = V_{DS} + 0V$$

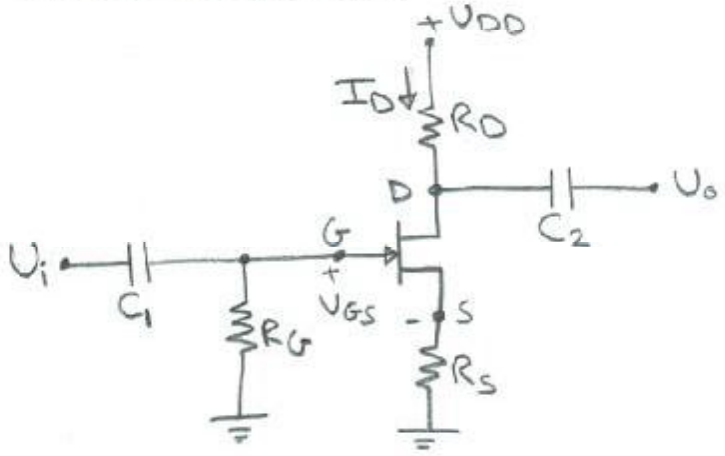
$$\therefore \boxed{V_D = V_{DS}}$$

$$V_{GS} = V_G - V_S \quad , \quad V_G = V_{GS} + V_S = V_{GS} + 0V$$

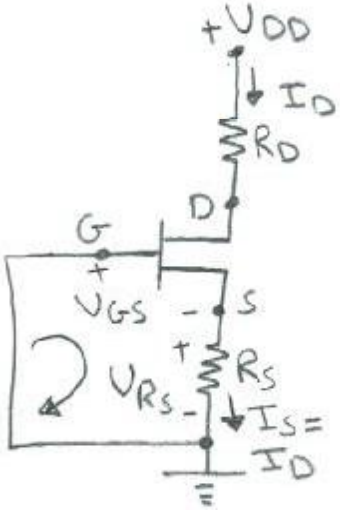
$$\boxed{V_G = V_{GS}}$$

Example 7.1

Self-Bias Configuration:



The network used for the dc analysis of the self-bias configuration is shown below:



$V_{R_S} = I_S R_S$ since $I_D = I_S$

$V_{R_S} = I_D R_S$

for the i/p loop :-

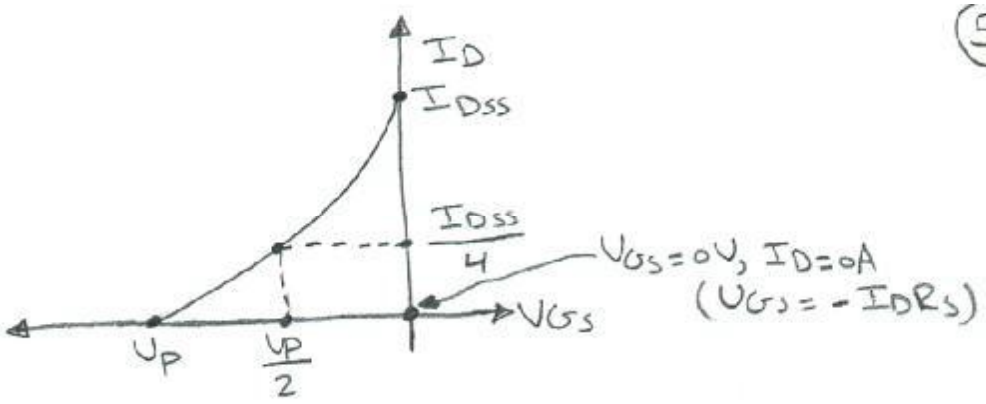
$-V_{GS} - V_{R_S} = 0$

$V_{GS} = -V_{R_S}$

$$\boxed{V_{GS} = -I_D R_S}$$

Using the graphical approach:

First draw the transfer curve.



Now draw the equation $V_{GS} = -I_D R_S$ on the same graph since they both relate the same variables I_D, V_{GS} to obtain the biasing levels.

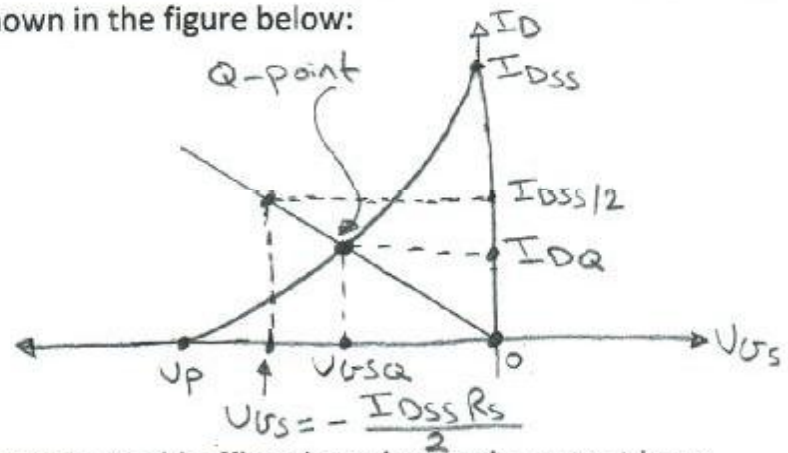
To draw the equation $V_{GS} = -I_D R_S$ which is a straight line, two points are required. The first two points is chosen for:

$I_D = 0 \Rightarrow V_{GS} = 0$

The second point is chosen for example $I_D = I_{DSS}\backslash 2$

$$V_{GS} = -I_D R_S = -\frac{I_{DSS} R_S}{2}$$

Then a straight line is drawn passing through these two points and the quiescent point is obtained at the intersection of the straight line plot and the c/c's curve as shown in the figure below:



Applying Kirchhoff's voltage law at the output loop:

$$V_{R_S} + V_{DS} + V_{R_D} - V_{DD} = 0$$

$$V_{DS} = V_{DD} - V_{R_S} - V_{R_D} = V_{DD} - I_S R_S - I_D R_D$$

$\because I_D = I_S$

$\therefore \boxed{V_{DS} = V_{DD} - I_D(R_S + R_D)}$

$$V_S = I_D R_S$$

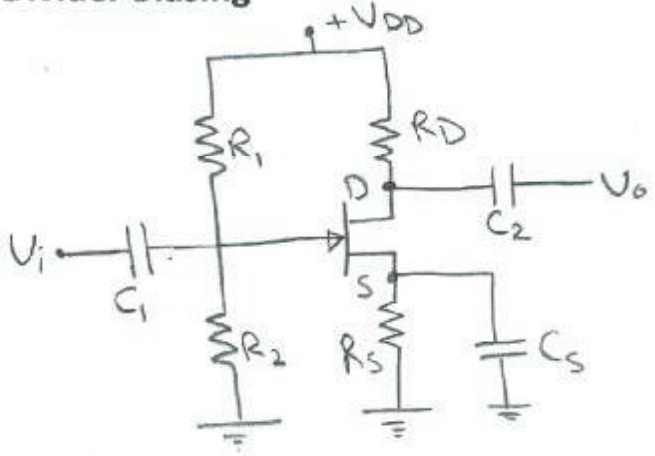
$$V_G = 0\,V$$

$$V_D = V_{DS} + V_S = V_{DD} - V_{RD}$$

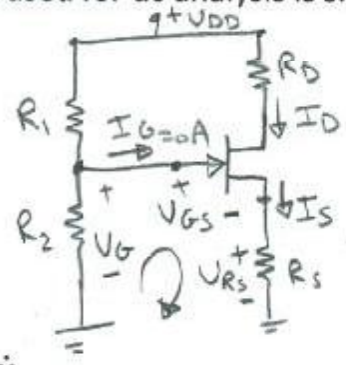
Example 7.2

Example 7.3

Voltage-Divider Biasing



The network used for dc analysis is shown below:



Since $I_G = 0$ ∴

$$\therefore I_{R_1} = I_{R_2}$$

$$V_G = \frac{V_{DD} * R_2}{R_1 + R_2}$$

Applying Kirchhoff's voltage law to the input (Gate-source) loop results in:

$V_G - V_{GS} - V_{R_S} = 0$

$V_{GS} = V_G - V_{R_S}$

$V_{R_S} = I_S R_S = I_D R_S$

$\boxed{V_{GS} = V_G - I_D R_S}$ which is an equation of a straight line.

To plot the equation $V_{GS} = V_G - I_D R_S$ two points are required:

First point if $I_D = 0mA$

$V_{GS} = V_G - 0$

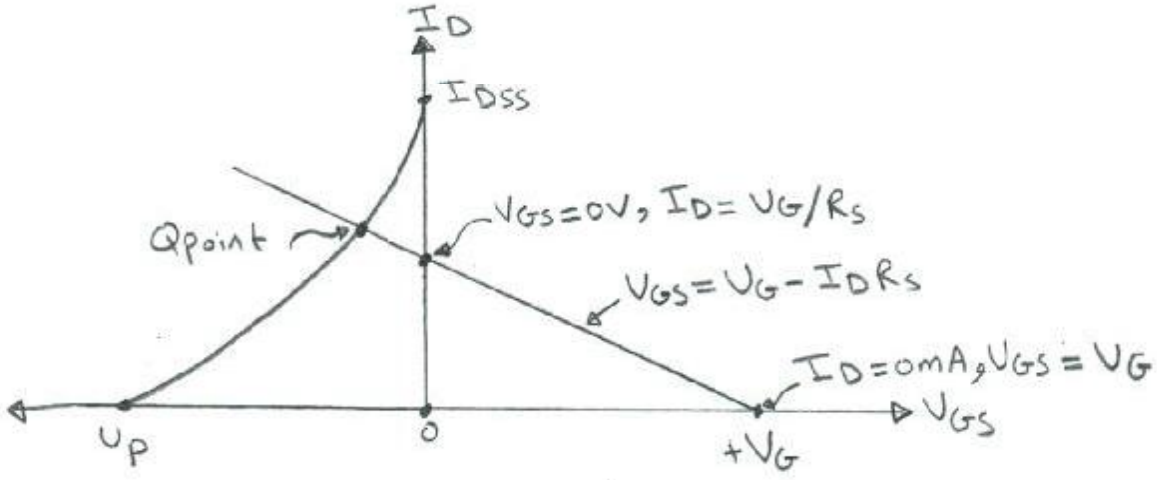
$\boxed{V_{GS} = V_G}$ $I_D = 0mA$

Second point if $V_{GS} = 0V$

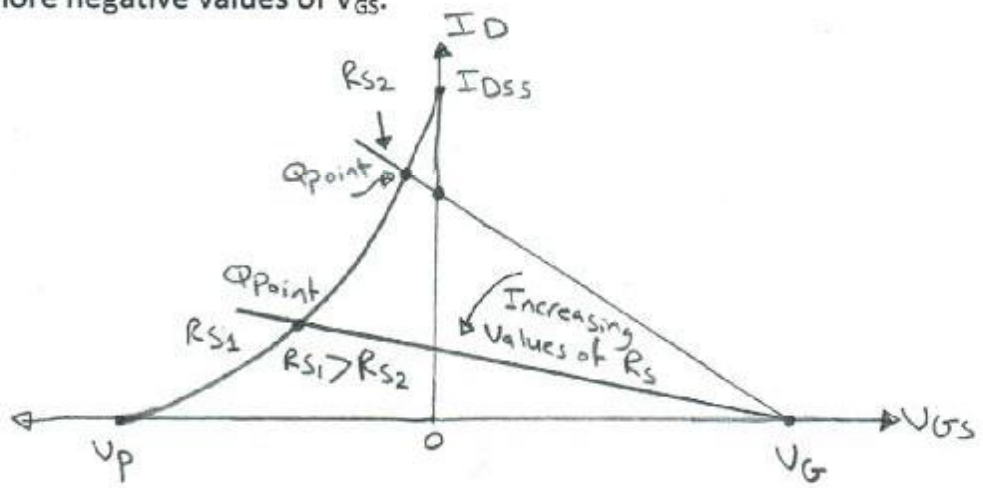
$0 = V_G - I_D R_S$

$\boxed{I_D = \frac{V_G}{R_S}}$ $V_{GS} = 0V$

Now the straight line can be drawn as shown below. The intersection of the straight line with the transfer curve defines the operating point (I_{DQ}, V_{GSQ}), as shown in the figure below:



The following figure shows the effect of R_S on the resulting Q-point. From the figure it is obvious that increasing values of R_S result in lower quiescent values of I_D and more negative values of V_{GS}.



Also

$$V_{DS} = V_{DD} - I_D (R_D + R_S)$$

$$V_D = V_{DD} - I_D R_D$$

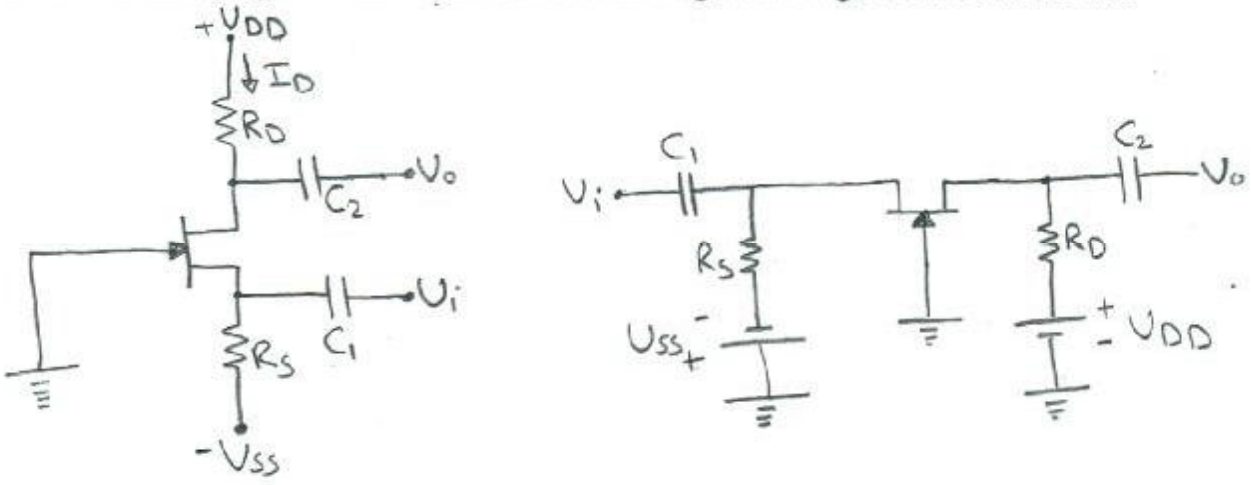
$$V_S = I_D R_S$$

$$I_{R_1} = I_{R_2} = \frac{V_{DD}}{R_1 + R_2}$$

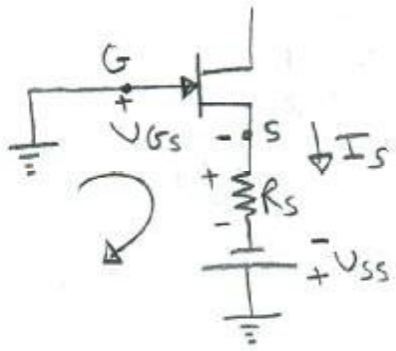
Example 7.5

Common-Gate Configuration:

In the following figure two versions of common-gate configurations are shown:



The network equation (equation relating I_D and V_{GS} from the network) can be found from the following figure:



Applying Kirchhoff's voltage law will result in:

$$-V_{GS} - I_S R_S + V_{SS} = 0$$

$$V_{GS} = V_{SS} - I_S R_S$$

$$I_S = I_D$$

$$\boxed{V_{GS} = V_{SS} - I_D R_S}$$

Applying the condition I_D = 0mA will result in:

$$V_{GS} = V_{SS} - (0) * R_S$$

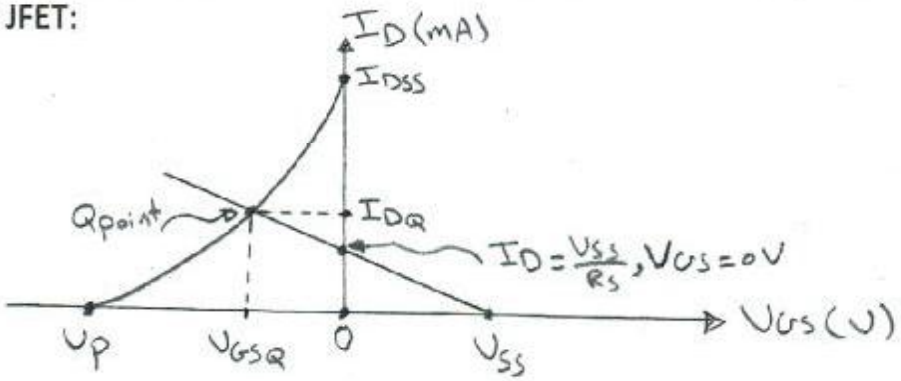
$$\boxed{V_{GS} = V_{SS}} \quad I_D = 0mA$$

Applying the condition V_{GS} = 0V will result in:

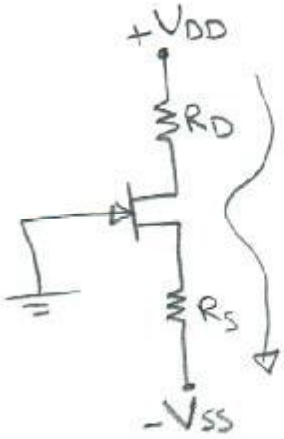
$$0 = V_{SS} - I_D R_S$$

$$\boxed{I_D = \frac{V_{SS}}{R_S}} \quad V_{GS} = 0V$$

The resulting load line is shown in the following figure intersecting the transfer curve for the JFET:



Applying Kirchhoff's voltage law across both sources of the output loop of the following figure will result in:



$$+V_{DD} - I_D R_D - V_{DS} - I_S R_S + V_{SS} = 0$$

Substituting $I_D = I_S$

$$+V_{DD} + V_{SS} - V_{DS} - I_D(R_D + R_S) = 0$$

$$\boxed{V_{DS} = V_{DD} + V_{SS} - I_D(R_D + R_S)}$$

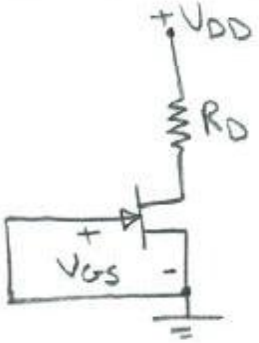
$$\boxed{V_D = V_{DD} - I_D R_D}$$

$$\boxed{V_S = -V_{SS} + I_D R_S}$$

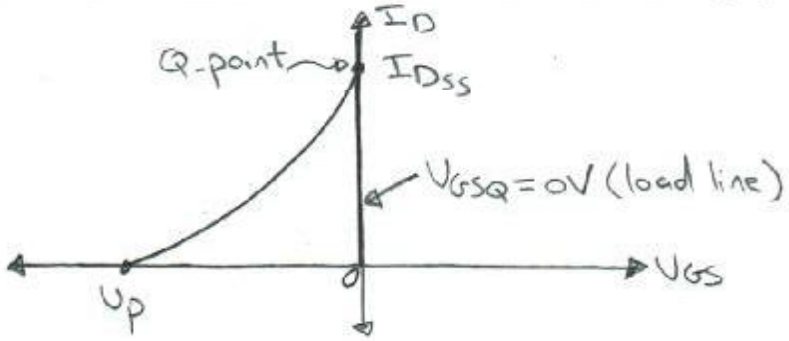
Example 7.6

Special Case: V_{GSQ} = 0V:

In the following figure V_{GS} = 0V by connecting the gate and source terminals to ground:



This will result in a vertical load line as shown in the following figure:



$\therefore I_{DQ} = I_{DSS}$ (the intersection of the load line and the transfer curve of the JFET).

Applying Kirchhoff's voltage law at the output:

$$V_{DD} - I_D R_D - V_{DS} = 0$$

$$V_{DS} = V_{DD} - I_D R_D$$

$$V_D = V_{DS}$$

$$V_S = 0V$$

Depletion-Type MOSFETs:

The analysis is the same as for the JFETs, the only difference is that MOSFETs permit operating points with positive V_{GS} values and levels of $I_D > I_{DSS}$.

Example 7.7

Example 7.8

Example 7.9

Example 7.10

Enhancement-Type MOSFETs:

The transfer c/c's is different for the enhancement type MOSFET. **For n-channel enhancement-type MOSFETs $I_D = 0mA$ for $V_{GS} < V_{th}$.**

And if $V_{GS} > V_{th}$ then:

$$I_D = k(V_{GS} - V_{th})^2$$

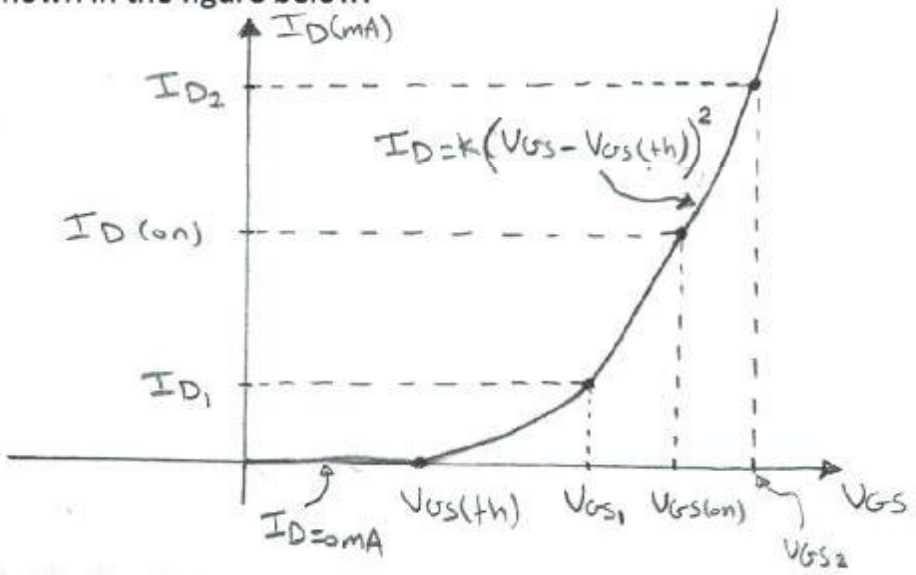
On specification sheets V_{th} is specified in addition to a level of I_D ($I_{D(on)}$) and its corresponding level of V_{GS} ($V_{GS(on)}$), therefore two points are already specified. To complete the transfer curve, the constant **k** must be determined so:

$$I_D = K(V_{GS} - V_{th})^2$$

$$I_{D(on)} = K(V_{GS(on)} - V_{th})^2$$

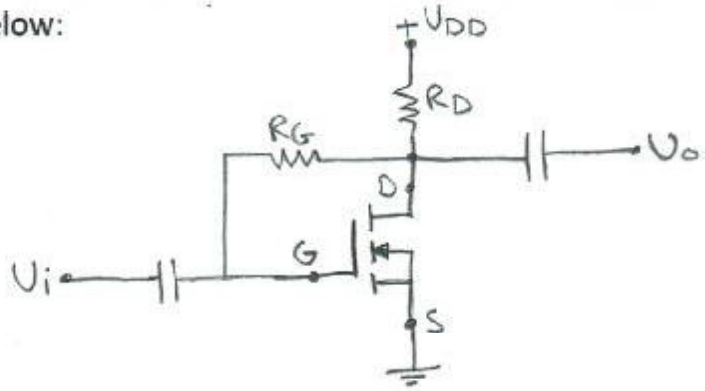
$$K = \frac{I_{D(on)}}{(V_{GS(on)} - V_{th})^2}$$

When k is known other points on the curve can be found to complete the transfer curve plot. Typically, a point between V_{th} and $V_{GS(on)}$ and one just greater than $V_{GS(on)}$ as shown in the figure below:

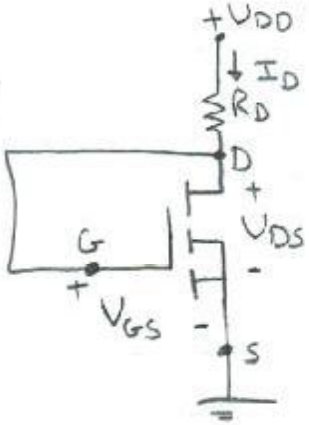


Feedback Biasing Arrangement:

A popular biasing arrangement for enhancement-type MOSFETs is shown in the figure below:



The dc equivalent of the network is shown below:



$V_D = V_G$

$$V_{DS} = V_{GS}$$

For the output circuit:

$$V_{DS} = V_{DD} - I_D R_D$$

$$\therefore V_{GS} = V_{DD} - I_D R_D$$

To plot the equation $V_{GS} = V_{DD} - I_D R_D$ two points are required:

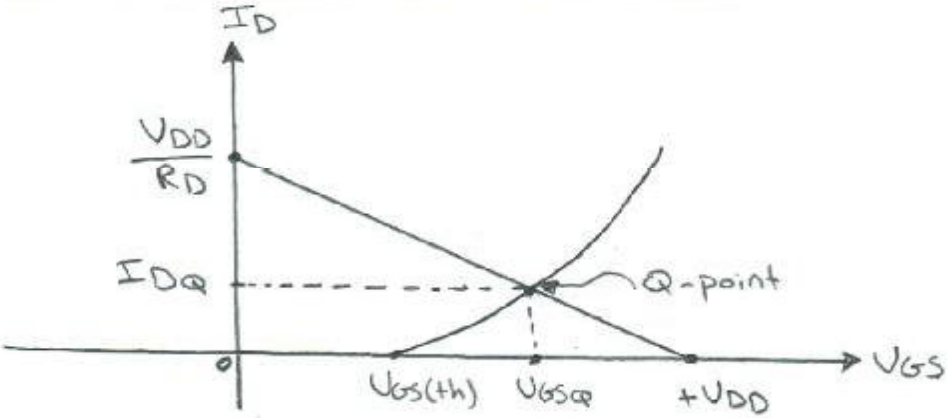
The first point if $I_D = 0mA$ results in:

$$V_{GS} = V_{DD} \quad I_D = 0mA$$

The second point if $V_{GS} = 0V$:

$$I_D = \frac{V_{DD}}{R_D} \quad V_{GS} = 0V$$

The plot of the load line and its intersection with the transfer curve is shown below with the resulting operating point (Q-point).

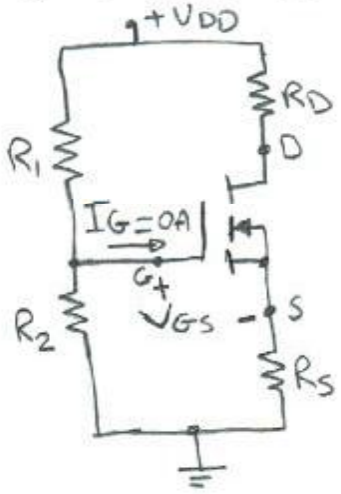


Example 7.11

Voltage-Divider Biasing Arrangement:

The d.c equivalent of the voltage divider is shown below:-

$$V_G = V_{DD}\frac{R_2}{R_1+R_2}$$



Applying Kirchhoff's voltage law results in:

$$V_G - V_{GS} - V_{RS} = 0$$

$$V_{GS} = V_G - V_{RS}$$

$$V_{GS} = V_G - I_D R_S$$ ← plot this equation and intersect with the transfer curve to obtain (I_{DQ}, V_{GSQ}).

For the output section:

$$V_{RS} + V_{DS} + V_{RD} - V_{DD} = 0$$

$$V_{DS} = V_{DD} - V_{RS} - V_{RD}$$

$$V_{DS} = V_{DD} - I_D(R_S + R_D)$$

Example 7.12

Combination Networks:

Example 7.13

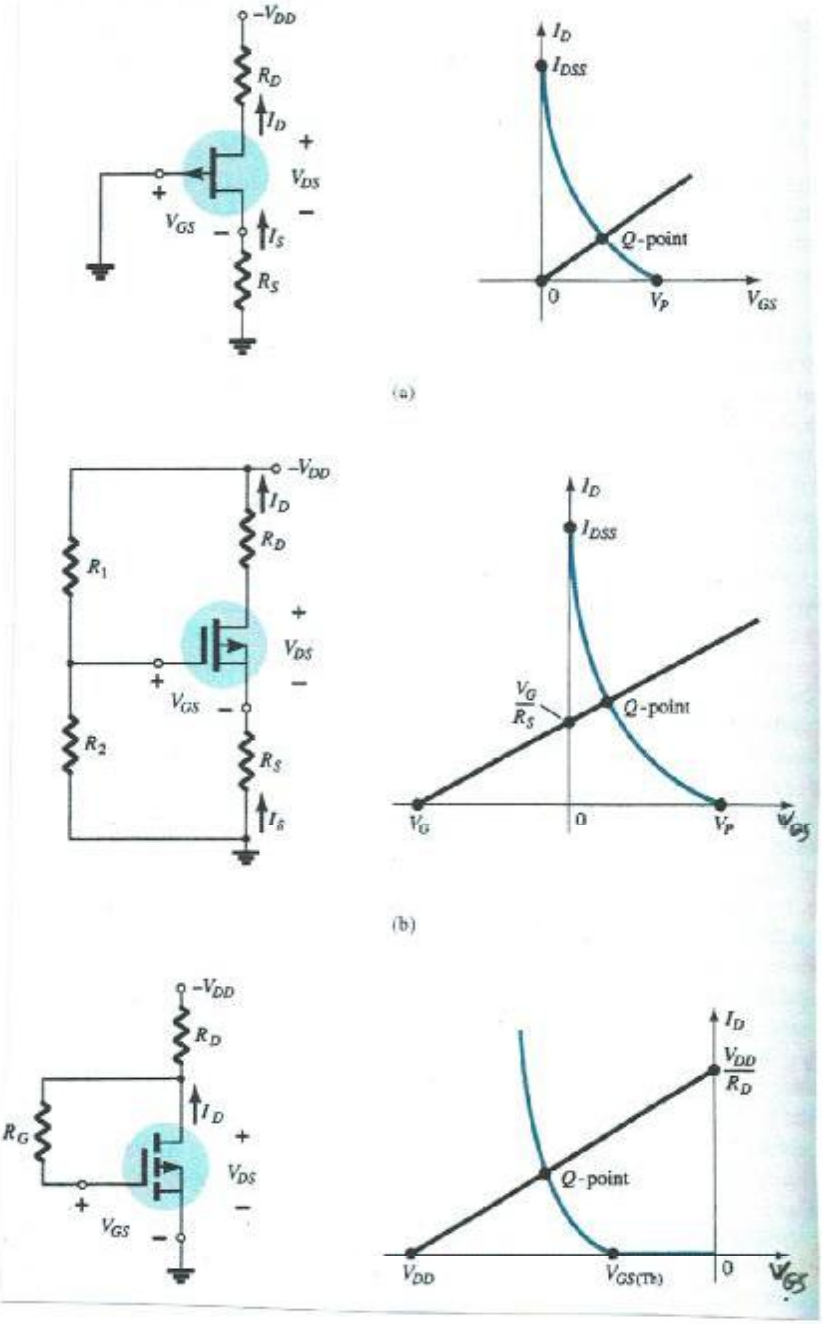
Example 7.14

Design:

Example 7.15, Example 7.16, Example 7.17

p-channel FETs:

For p-channel FETs a mirror image of the transfer curve is employed, and the defined current directions are reversed as shown below:



Example 7.18

Shorthand Method

Since the transfer curve must be plotted so frequently, it would be quite advantageous to have a shorthand method for plotting the curve in the quickest, most efficient manner while maintaining an acceptable degree of accuracy. The format of Eq. (6.3) is such that specific levels of V_{GS} will result in levels of I_D that can be memorized to provide the plot points needed to sketch the transfer curve. If we specify V_{GS} to be one-half the pinch-off value V_P, the resulting level of I_D will be the following, as determined by Shockley's equation:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$= I_{DSS}\left(\frac{1 - V_P/2}{V_P}\right)^2 = I_{DSS}\left(1 - \frac{1}{2}\right)^2 = I_{DSS}(0.5)^2$$

$$= I_{DSS}(0.25)$$

and

$$\boxed{I_D = \left.\frac{I_{DSS}}{4}\right|_{V_{GS} = V_P/2}} \qquad \textbf{(6.9)}$$

Now it is important to realize that Eq. (6.9) is not for a particular level of V_P. It is a general equation for any level of V_P as long as $V_{GS} = V_P/2$. The result specifies that the drain current will always be one-fourth the saturation level I_{DSS} as long as the gate-to-source voltage is one-half the pinch-off value. Note the level of I_D for $V_{GS} = V_P/2 = -4\,\text{V}/2 = -2\,\text{V}$ in Fig. 6.17.

If we choose $I_D = I_{DSS}/2$ and substitute into Eq. (6.8), we find that

$$V_{GS} = V_P\left(1 - \sqrt{\frac{I_D}{I_{DSS}}}\right)$$

$$= V_P\left(1 - \sqrt{\frac{I_{DSS}/2}{I_{DSS}}}\right) = V_P(1 - \sqrt{0.5}) = V_P(0.293)$$

and

$$\boxed{V_{GS} \cong 0.3V_P\big|_{I_D = I_{DSS}/2}} \qquad \textbf{(6.10)}$$

Additional points can be determined, but the transfer curve can be sketched to a satisfactory level of accuracy simply using the four plot points defined above and reviewed in Table 6.1. In fact, in the analysis of Chapter 7, a maximum of four plot points are used to sketch the transfer curves. On most occasions using just the plot point defined by $V_{GS} = V_P/2$ and the axis intersections at I_{DSS} and V_P will provide a curve accurate enough for most calculations.

TABLE 6.1
V_{GS} Versus I_D Using Shockley's Equation

V_{GS}	I_D
0	I_{DSS}
$0.3V_P$	$I_{DSS}/2$
$0.5V_P$	$I_{DSS}/4$
V_P	0 mA

EXAMPLE 6.1 Sketch the transfer curve defined by $I_{DSS} = 12\,\text{mA}$ and $V_P = -6\,\text{V}$.

Solution: Two plot points are defined by

$$I_{DSS} = \mathbf{12\,mA} \quad \text{and} \quad V_{GS} = \mathbf{0\,V}$$

and

$$I_D = \mathbf{0\,mA} \quad \text{and} \quad V_{GS} = \mathbf{V_P}$$

At $V_{GS} = V_P/2 = -6\,\text{V}/2 = \mathbf{-3\,V}$ the drain current is determined by $I_D = I_{DSS}/4 = 12\,\text{mA}/4 = \mathbf{3\,mA}$. At $I_D = I_{DSS}/2 = 12\,\text{mA}/2 = \mathbf{6\,mA}$ the gate-to-source voltage is determined by $V_{GS} \cong 0.3V_P = 0.3(-6\,\text{V}) = \mathbf{-1.8\,V}$. All four plot points are well defined on Fig. 6.18 with the complete transfer curve.

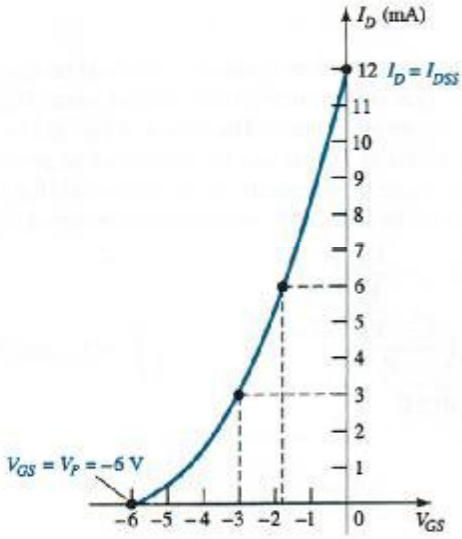


FIG. 6.18
Transfer curve for Example 6.1.

For p-channel devices Shockley's equation (6.3) can still be applied exactly as it appears. In this case, both V_P and V_{GS} will be positive and the curve will be the mirror image of the transfer curve obtained with an n-channel and the same limiting values.

EXAMPLE 6.2 Sketch the transfer curve for a p-channel device with $I_{DSS} = 4$ mA and $V_P = 3$ V.

Solution: At $V_{GS} = V_P/2 = 3\text{ V}/2 = \mathbf{1.5\text{ V}}$, $I_D = I_{DSS}/4 = 4\text{ mA}/4 = \mathbf{1\text{ mA}}$. At $I_D = I_{DSS}/2 = 4\text{ mA}/2 = \mathbf{2\text{ mA}}$, $V_{GS} = 0.3V_P = 0.3(3\text{ V}) = \mathbf{0.9\text{ V}}$. Both plot points appear in Fig. 6.19 along with the points defined by I_{DSS} and V_P.

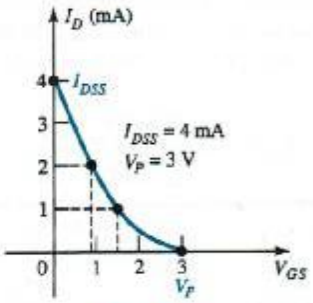


FIG. 6.19
Transfer curve for the p-channel device of Example 6.2.

Mathcad

Using Mathcad, we will now plot Shockley's equation using the **X-Y plot operator**. The plot operator can be selected using the **Graph = X-Y Plot** under the **Insert** option on the menu bar.

Once the plot is chosen, Mathcad will create a graph with placeholders on each axis as shown in Fig. 6.20. To plot Shockley's equation, first select the placeholder in the middle of the horizontal axis and enter the horizontal variable **VGS**. Then establish a range for **VGS** by first typing **VGS** followed by a colon and the range of values. The range of values is

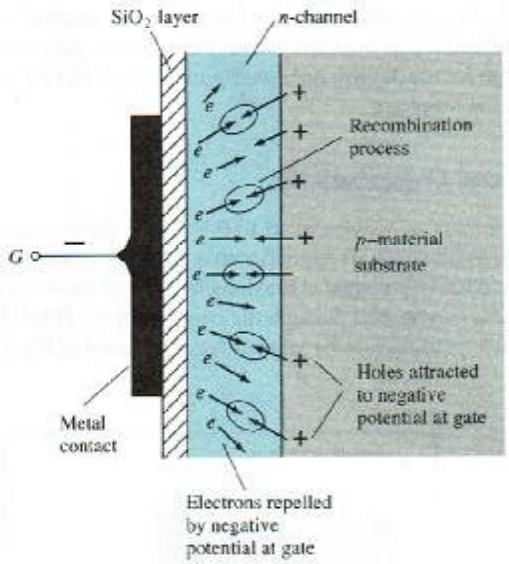


FIG. 6.30
Reduction in free carriers in a channel due to a negative potential at the gate terminal.

magnitude of the negative bias established by V_{GS}, a level of recombination between electrons and holes will occur that will reduce the number of free electrons in the *n*-channel available for conduction. The more negative the bias, the higher is the rate of recombination. The resulting level of drain current is therefore reduced with increasing negative bias for V_{GS}, as shown in Fig. 6.29 for $V_{GS} = -1$ V, -2 V, and so on, to the pinch-off level of -6 V. The resulting levels of drain current and the plotting of the transfer curve proceed exactly as described for the JFET.

For positive values of V_{GS}, the positive gate will draw additional electrons (free carriers) from the *p*-type substrate due to the reverse leakage current and establish new carriers through the collisions resulting between accelerating particles. As the gate-to-source voltage continues to increase in the positive direction, Fig. 6.29 reveals that the drain current will increase at a rapid rate for the reasons listed above. The vertical spacing between the $V_{GS} = 0$ V and $V_{GS} = +1$ V curves of Fig. 6.29 is a clear indication of how much the current has increased for the 1-V change in V_{GS}. Due to the rapid rise, the user must be aware of the maximum drain current rating since it could be exceeded with a positive gate voltage. That is, for the device of Fig. 6.29, the application of a voltage $V_{GS} = +4$ V would result in a drain current of 22.2 mA, which could possibly exceed the maximum rating (current or power) for the device. As revealed above, the application of a positive gate-to-source voltage has "enhanced" the level of free carriers in the channel compared to that encountered with $V_{GS} = 0$ V. For this reason the region of positive gate voltages on the drain or transfer characteristics is often referred to as the *enhancement region*, with the region between cutoff and the saturation level of I_{DSS} referred to as the *depletion region*.

It is particularly interesting and helpful that Shockley's equation will continue to be applicable for the depletion-type MOSFET characteristics in both the depletion and enhancement regions. For both regions, it is simply necessary that the proper sign be included with V_{GS} in the equation and the sign be carefully monitored in the mathematical operations.

EXAMPLE 6.3 Sketch the transfer characteristics for an *n*-channel depletion-type MOSFET with $I_{DSS} = 10$ mA and $V_P = -4$ V.

Solution:

$$\text{At } V_{GS} = 0 \text{ V}, \quad I_D = I_{DSS} = 10 \text{ mA}$$
$$V_{GS} = V_P = -4 \text{ V}, \quad I_D = 0 \text{ mA}$$
$$V_{GS} = \frac{V_P}{2} = \frac{-4 \text{ V}}{2} = -2 \text{ V}, \quad I_D = \frac{I_{DSS}}{4} = \frac{10 \text{ mA}}{4} = 2.5 \text{ mA}$$

and at $I_D = \frac{I_{DSS}}{2}$,

$$V_{GS} = 0.3V_P = 0.3(-4\text{ V}) = -1.2\text{ V}$$

all of which appear in Fig. 6.31.

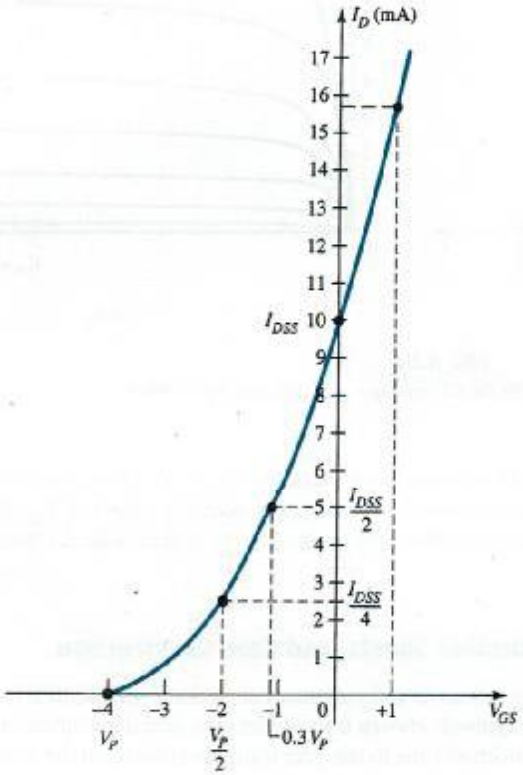


FIG. 6.31
Transfer characteristics for an n-channel depletion-type MOSFET with $I_{DSS} = 10$ mA and $V_P = -4$ V.

Before plotting the positive region of V_{GS}, keep in mind that I_D increases very rapidly with increasing positive values of V_{GS}. In other words, be conservative with the choice of values to be substituted into Shockley's equation. In this case, we try +1 V as follows:

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$= (10\text{ mA})\left(1 - \frac{+1\text{ V}}{-4\text{ V}}\right)^2 = (10\text{ mA})\,(1 + 0.25)^2 = (10\text{ mA})\,(1.5625)$$

$$\cong 15.63\text{ mA}$$

which is sufficiently high to finish the plot.

p-Channel Depletion-Type MOSFET

The construction of a *p*-channel depletion-type MOSFET is exactly the reverse of that appearing in Fig. 6.27. That is, there is now an *n*-type substrate and a *p*-type channel, as shown in Fig. 6.32a. The terminals remain as identified, but all the voltage polarities and the current directions are reversed, as shown in the same figure. The drain characteristics would appear exactly as in Fig. 6.29, but with V_{DS} having negative values, I_D having positive values as indicated (since the defined direction is now reversed), and V_{GS} having the opposite polarities as shown in Fig. 6.32c. The reversal in V_{GS} will result in a mirror image (about the I_D axis) for the transfer characteristics as shown in Fig. 6.32b. In other words,

EXAMPLE 7.1 Determine the following for the network of Fig. 7.6:

a. V_{GSQ}.
b. I_{DQ}.
c. V_{DS}.
d. V_D.
e. V_G.
f. V_S.

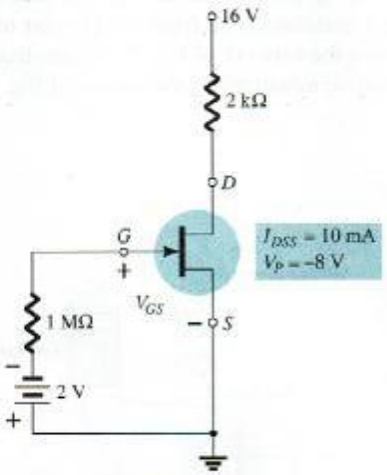


FIG. 7.6
Example 7.1.

Solution:

Mathematical Approach

a. $V_{GS_Q} = -V_{GG} = \mathbf{-2\ V}$

b. $$I_{D_Q} = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = 10\text{ mA}\left(1 - \frac{-2\text{ V}}{-8\text{ V}}\right)^2$$
$$= 10\text{ mA}(1 - 0.25)^2 = 10\text{ mA}(0.75)^2 = 10\text{ mA}(0.5625)$$
$$= \mathbf{5.625\ mA}$$

c. $$V_{DS} = V_{DD} - I_D R_D = 16\text{ V} - (5.625\text{ mA})(2\text{ k}\Omega)$$
$$= 16\text{ V} - 11.25\text{ V} = \mathbf{4.75\ V}$$

d. $V_D = V_{DS} = \mathbf{4.75\ V}$

e. $V_G = V_{GS} = \mathbf{-2\ V}$

f. $V_S = \mathbf{0\ V}$

Graphical Approach The resulting Shockley curve and the vertical line at $V_{GS} = -2$ V are provided in Fig. 7.7. It is certainly difficult to read beyond the second place without

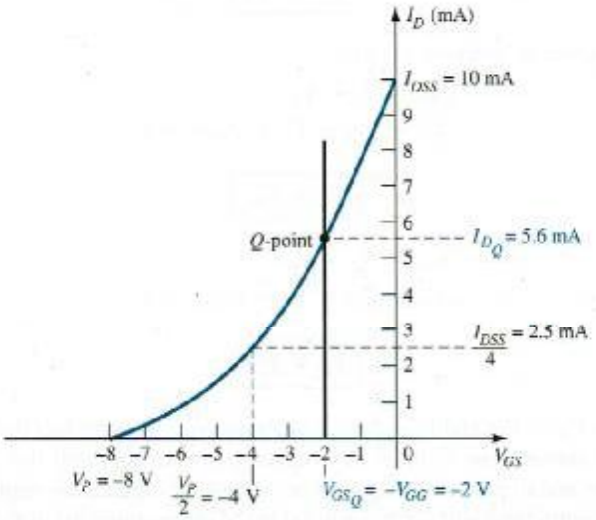


FIG. 7.7
Graphical solution for the network of Fig. 7.6.

significantly increasing the size of the figure, but a solution of 5.6 mA from the graph of Fig. 7.7 is quite acceptable.

a. Therefore,

$$V_{GS_Q} = -V_{GG} = \mathbf{-2\,V}$$

b. $I_{D_Q} = \mathbf{5.6\,mA}$

c. $V_{DS} = V_{DD} - I_D R_D = 16\,\text{V} - (5.6\,\text{mA})(2\,\text{k}\Omega)$
$= 16\,\text{V} - 11.2\,\text{V} = \mathbf{4.8\,V}$

d. $V_D = V_{DS} = \mathbf{4.8\,V}$

e. $V_G = V_{GS} = \mathbf{-2\,V}$

f. $V_S = \mathbf{0\,V}$

The results clearly confirm the fact that the mathematical and graphical approaches generate solutions that are quite close.

7.3 SELF-BIAS CONFIGURATION

The self-bias configuration eliminates the need for two dc supplies. The controlling gate-to-source voltage is now determined by the voltage across a resistor R_S introduced in the source leg of the configuration as shown in Fig. 7.8.

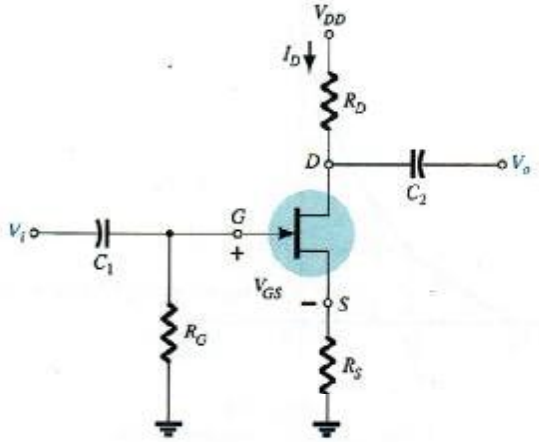


FIG. 7.8
JFET self-bias configuration.

For the dc analysis, the capacitors can again be replaced by "open circuits" and the resistor R_G replaced by a short-circuit equivalent since $I_G = 0\,\text{A}$. The result is the network of Fig. 7.9 for the important dc analysis.

The current through R_S is the source current I_S, but $I_S = I_D$ and

$$V_{R_S} = I_D R_S$$

For the indicated closed loop of Fig. 7.9, we find that

$$-V_{GS} - V_{R_S} = 0$$

and

$$V_{GS} = -V_{R_S}$$

or

$$\boxed{V_{GS} = -I_D R_S} \qquad (7.10)$$

Note in this case that V_{GS} is a function of the output current I_D and not fixed in magnitude as occurred for the fixed-bias configuration.

Equation (7.10) is defined by the network configuration, and Shockley's equation relates the input and output quantities of the device. Both equations relate the same two variables, permitting either a mathematical or a graphical solution.

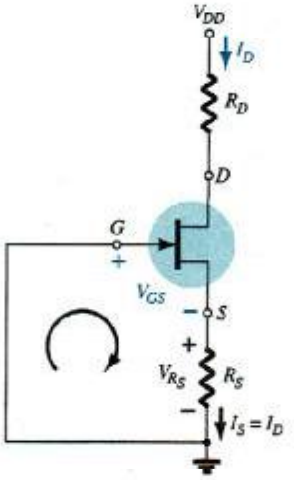


FIG. 7.9
DC analysis of the self-bias configuration.

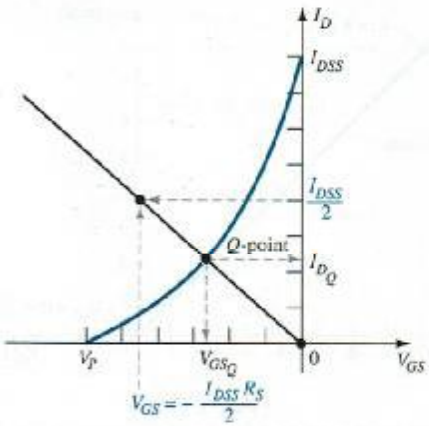


FIG. 7.11
Sketching the self-bias line.

but $$I_D = I_S$$

and $$V_{DS} = V_{DD} - I_D(R_S + R_D) \tag{7.11}$$

In addition,

$$V_S = I_D R_S \tag{7.12}$$

$$V_G = 0\,\text{V} \tag{7.13}$$

and $$V_D = V_{DS} + V_S = V_{DD} - V_{R_D} \tag{7.14}$$

EXAMPLE 7.2 Determine the following for the network of Fig. 7.12:

a. V_{GS_Q}.
b. I_{D_Q}.
c. V_{DS}.
d. V_S.
e. V_G.
f. V_D.

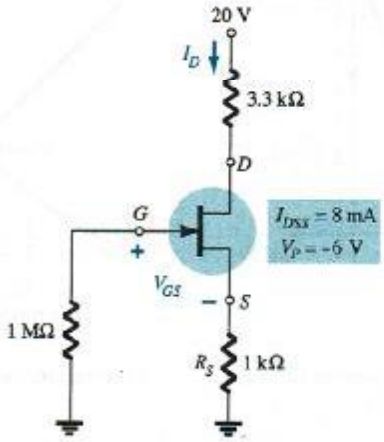


FIG. 7.12
Example 7.2.

Solution:

a. The gate-to-source voltage is determined by

$$V_{GS} = -I_D R_S$$

Choosing $I_D = 4$ mA, we obtain

$$V_{GS} = -(4\,\text{mA})(1\,\text{k}\Omega) = -4\,\text{V}$$

The result is the plot of Fig. 7.13 as defined by the network.

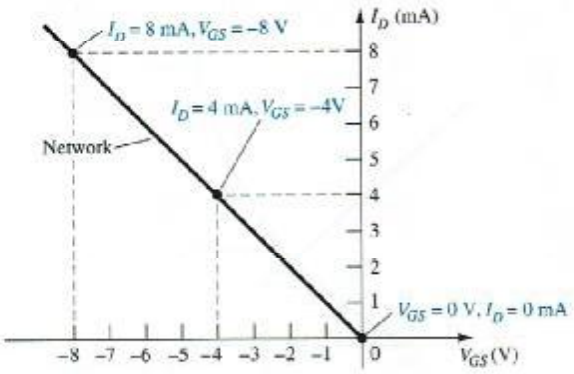


FIG. 7.13
Sketching the self-bias line for the network of Fig. 7.12.

If we happen to choose $I_D = 8$ mA, the resulting value of V_{GS} would be -8 V, as shown on the same graph. In either case, the same straight line will result, clearly demonstrating that any appropriate value of I_D can be chosen as long as the corresponding value of V_{GS} as determined by Eq. (7.10) is employed. In addition, keep in mind that the value of V_{GS} could be chosen and the value of I_D calculated with the same resulting plot.

For Shockley's equation, if we choose $V_{GS} = V_P/2 = -3$ V, we find that $I_D = I_{DSS}/4 = 8$ mA$/4 = 2$ mA, and the plot of Fig. 7.14 will result, representing the characteristics of the device. The solution is obtained by superimposing the network characteristics defined by Fig. 7.13 on the device characteristics of Fig. 7.14 and finding the point of intersection of the two as indicated on Fig. 7.15. The resulting operating point results in a quiescent value of gate-to-source voltage of

$$V_{GS_Q} = \mathbf{-2.6\ V}$$

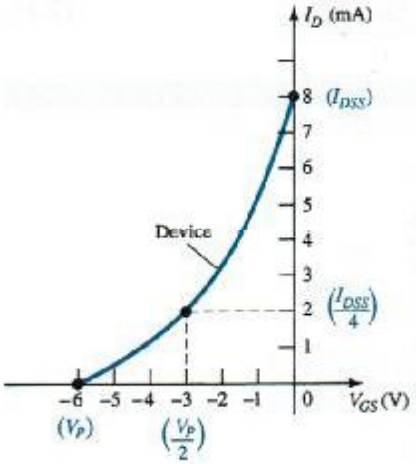


FIG. 7.14
Sketching the device characteristics for the JFET of Fig. 7.12.

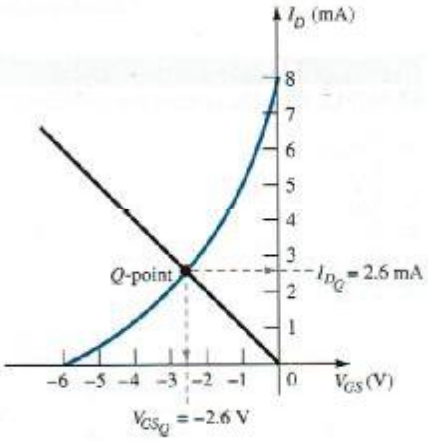


FIG. 7.15
Determining the Q-point for the network of Fig. 7.12.

b. At the quiescent point

$$I_{D_Q} = \mathbf{2.6\ mA}$$

c. Eq. (7.11): $V_{DS} = V_{DD} - I_D(R_S + R_D)$
$= 20\text{ V} - (2.6\text{ mA})(1\text{ k}\Omega + 3.3\text{ k}\Omega)$
$= 20\text{ V} - 11.18\text{ V}$
$= \mathbf{8.82\ V}$

d. Eq. (7.12): $V_S = I_D R_S$
$= (2.6\text{ mA})(1\text{ k}\Omega)$
$= \mathbf{2.6\ V}$

e. Eq. (7.13): $V_G = \mathbf{0\ V}$

f. Eq. (7.14): $V_D = V_{DS} + V_S = 8.82\ \text{V} + 2.6\ \text{V} = \mathbf{11.42\ V}$

or $V_D = V_{DD} - I_D R_D = 20\ \text{V} - (2.6\ \text{mA})(3.3\ \text{k}\Omega) = \mathbf{11.42\ V}$

Mathcad

Mathcad will now be used to find the quiescent conditions for Example 7.2 using a process described in detail in Section 2.2. The two simultaneous equations that defined the Q-point for the network of Fig. 7.12 are

$$I_D = -\frac{V_{GS}}{R_S} = -\frac{V_{GS}}{1\ \text{k}\Omega}$$

and

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = 8\ \text{mA}\left(1 - \frac{V_{GS}}{-6\ \text{V}}\right)^2$$

After calling up Mathcad, we must first provide guesses for the two variables I_D and V_{GS}. The chosen values are 8 mA and −5 V, respectively. Each is entered by first entering the variable followed by **Shift:**. Next, the word **Given** must be entered, followed by the two simultaneous equations using the equal sign obtained from **Ctrl** =. Finally, the variables to be determined must be defined by **Find (ID, VGS)** as shown in Fig. 7.16. The results will appear once the equal sign is entered.

Mathcad returns a value of −2.59 V for **VGS**, which is very close to the calculated level of −2.6 V. In addition, the current of 2.59 mA is very close to the calculated level of 2.6 mA.

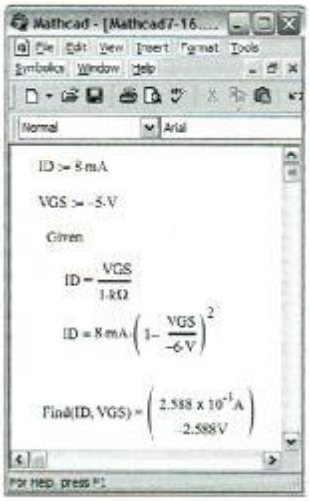


FIG. 7.16
Determining the quiescent point of operation for the network of Example 7.2.

EXAMPLE 7.3 Find the quiescent point for the network of Fig. 7.12 if:

a. $R_S = 100\ \Omega$.

b. $R_S = 10\ \text{k}\Omega$.

Solution: Note Fig. 7.17.

a. With the I_D scale,

$$I_{D_Q} \cong \mathbf{6.4\ mA}$$

From Eq. (7.10),

$$V_{GS_Q} \cong \mathbf{-0.64\ V}$$

b. With the V_{GS} scale,

$$V_{GS_Q} \cong \mathbf{-4.6\ V}$$

From Eq. (7.10),

$$I_{D_Q} \cong \mathbf{0.46\ mA}$$

In particular, note how lower levels of R_S bring the load line of the network closer to the I_D axis, whereas increasing levels of R_S bring the load line closer to the V_{GS} axis.

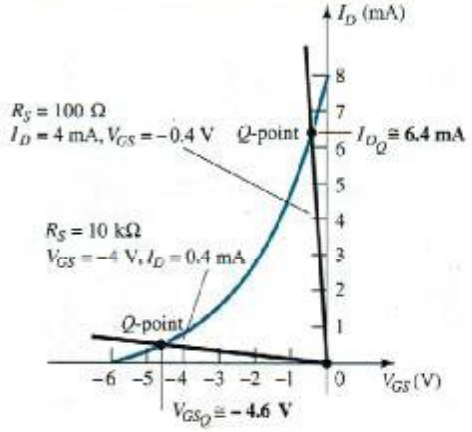


FIG. 7.17
Example 7.3.

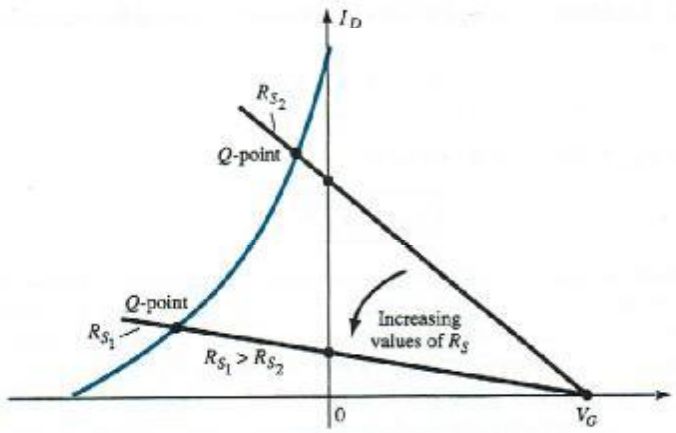


FIG. 7.21
Effect of R_S on the resulting Q-point.

shown in Fig. 7.21. It is fairly obvious from Fig. 7.24 that:

Increasing values of R_s result in lower quiescent values of I_D and more negative values of V_{GS}.

Once the quiescent values of I_{D_Q} and V_{GS_Q} are determined, the remaining network analysis can be performed in the usual manner. That is,

$$V_{DS} = V_{DD} - I_D(R_D + R_S) \tag{7.19}$$

$$V_D = V_{DD} - I_D R_D \tag{7.20}$$

$$V_S = I_D R_S \tag{7.21}$$

$$I_{R_1} = I_{R_2} = \frac{V_{DD}}{R_1 + R_2} \tag{7.22}$$

EXAMPLE 7.5 Determine the following for the network of Fig. 7.22:

a. I_{D_Q} and V_{GS_Q}.
b. V_D.
c. V_S.
d. V_{DS}.
e. V_{DG}.

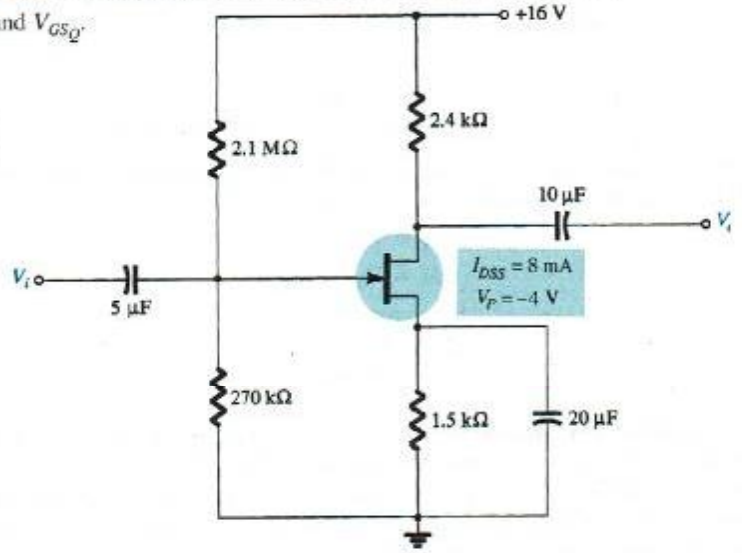


FIG. 7.22
Example 7.5.

Solution:

a. For the transfer characteristics, if $I_D = I_{DSS}/4 = 8\text{ mA}/4 = 2\text{ mA}$, then $V_{GS} = V_P/2 = -4\text{ V}/2 = -2\text{ V}$. The resulting curve representing Shockley's equation appears in Fig. 7.23. The network equation is defined by

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2}$$

$$= \frac{(270\text{ k}\Omega)(16\text{ V})}{2.1\text{ M}\Omega + 0.27\text{ M}\Omega}$$

$$= 1.82\text{ V}$$

and

$$V_{GS} = V_G - I_D R_S$$

$$= 1.82\text{ V} - I_D(1.5\text{ k}\Omega)$$

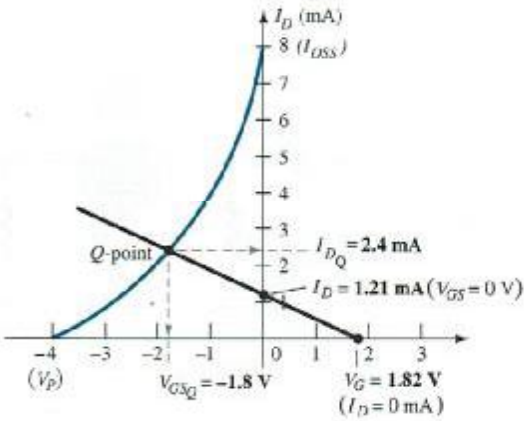


FIG. 7.23
Determining the Q-point for the network of Fig. 7.22.

When $I_D = 0\text{ mA}$,

$$V_{GS} = +1.82\text{ V}$$

When $V_{GS} = 0\text{ V}$,

$$I_D = \frac{1.82\text{ V}}{1.5\text{ k}\Omega} = 1.21\text{ mA}$$

The resulting bias line appears on Fig. 7.23 with quiescent values of

$$I_{D_Q} = \mathbf{2.4\text{ mA}}$$

and

$$V_{GS_Q} = \mathbf{-1.8\text{ V}}$$

b. $V_D = V_{DD} - I_D R_D$

$= 16\text{ V} - (2.4\text{ mA})(2.4\text{ k}\Omega)$

$= \mathbf{10.24\text{ V}}$

c. $V_S = I_D R_S = (2.4\text{ mA})(1.5\text{ k}\Omega)$

$= \mathbf{3.6\text{ V}}$

d. $V_{DS} = V_{DD} - I_D(R_D + R_S)$

$= 16\text{ V} - (2.4\text{ mA})(2.4\text{ k}\Omega + 1.5\text{ k}\Omega)$

$= \mathbf{6.64\text{ V}}$

or $V_{DS} = V_D - V_S = 10.24\text{ V} - 3.6\text{ V}$

$= \mathbf{6.64\text{ V}}$

e. Although seldom requested, the voltage V_{DG} can easily be determined using

$$V_{DG} = V_D - V_G$$
$$= 10.24\,\text{V} - 1.82\,\text{V}$$
$$= \mathbf{8.42\,V}$$

7.5 COMMON-GATE CONFIGURATION

The next configuration is one in which the gate terminal is grounded and the input signal typically applied to the source terminal and the output signal obtained at the drain terminal as shown in Fig. 7.24a. The network can also be drawn as shown in Fig. 7.24b.

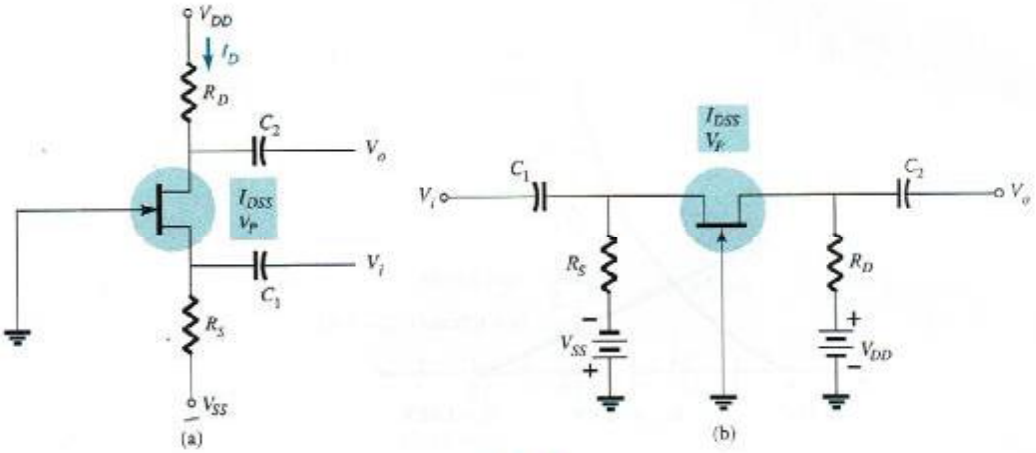


FIG. 7.24
Two versions of the common-gate configuration.

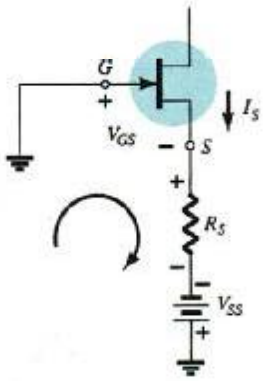


FIG. 7.25
Determining the network equation for the configuration of Fig. 7.24.

The network equation can be determined using Fig. 7.25.

Applying Kirchhoff's voltage law in the direction shown in Fig. 7.25 will result in

$$-V_{GS} - I_S R_S + V_{SS} = 0$$

and
$$V_{GS} = V_{SS} - I_S R_S$$

but
$$I_S = I_D$$

so
$$\boxed{V_{GS} = V_{SS} - I_D R_S} \qquad (7.23)$$

Applying the condition $I_D = 0\,\text{mA}$ to Eq. 7.23 will result in

$$V_{GS} = V_{SS} - (0)R_S$$

and
$$\boxed{V_{GS} = V_{SS}|_{I_D = 0\text{mA}}} \qquad (7.24)$$

Applying the condition $V_{GS} = 0\,\text{V}$ to Eq. 7.23 will result in

$$0 = V_{SS} - I_D R_S$$

and
$$\boxed{I_D = \left.\frac{V_{SS}}{R_S}\right|_{V_{GS}=0\,\text{V}}} \qquad (7.25)$$

The resulting load-line appears in Fig. 7.26 intersecting the transfer curve for the JFET as shown in the figure.

The resulting intersection defines the operating current I_{D_Q} and voltage V_{D_Q} for the network as also indicated in the network.

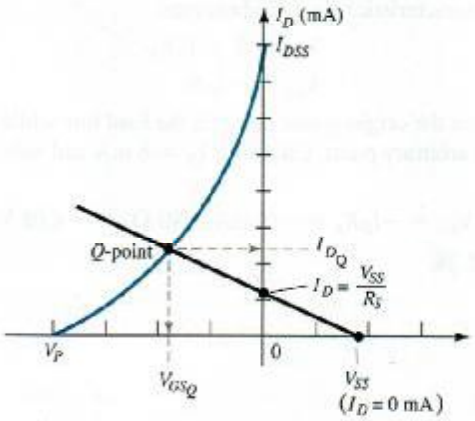


FIG. 7.26
Determining the Q-point for the network of Fig. 7.25.

Applying Kirchhoff's voltage law across both sources of Fig. 7.24a or Fig. 7.24b will result in

$$+V_{DD} - I_D R_D - V_{DS} - I_S R_S + V_{SS} = 0$$

Substituting $I_S = I_D$ we have

$$+V_{DD} + V_{SS} - V_{DS} - I_D(R_D + R_S) = 0$$

so that
$$\boxed{V_{DS} = V_{DD} + V_{SS} - I_D(R_D + R_S)} \quad \textbf{(7.26)}$$

with
$$\boxed{V_D = V_{DD} - I_D R_D} \quad \textbf{(7.27)}$$

and
$$\boxed{V_S = -V_{SS} + I_D R_S} \quad \textbf{(7.28)}$$

EXAMPLE 7.6 Determine the following for the common-gate configuration of Fig. 7.27:

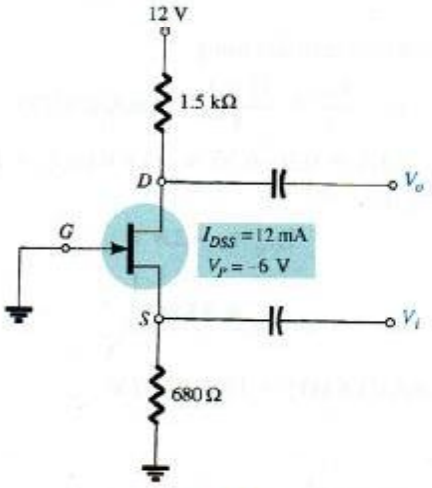


FIG. 7.27
Example 7.6.

Solution: Even though V_{SS} is not present in this common-gate configuration the equations derived above can still be used by simply substituting $V_{SS} = 0$ V into each equation in which it appears.

a. For the transfer characteristics Eq. 7.23 becomes

$$V_{GS} = 0 - I_D R_S$$

and

$$V_{GS} = -I_D R_S$$

For this equation the origin is one point on the load line while the other must be determined at some arbitrary point. Choosing $I_D = 6$ mA and solving for V_{GS} will result in the following:

$$V_{GS} = -I_D R_S = -(6\text{ mA})(680\ \Omega) = -4.08\text{ V}$$

as shown in Fig. 7.28.

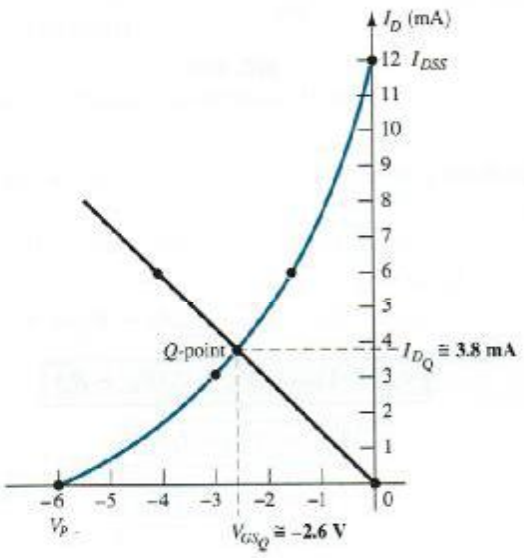


FIG. 7.28
Determining the Q-point for the network of Fig. 7.27.

The device transfer curve is sketched using

$$I_D = \frac{I_{DSS}}{4} = \frac{12\text{ mA}}{4} = 3\text{ mA}(\text{at } V_P/2)$$

and

$$V_{GS} = 0.3V_P = 0.3(-6\text{ V}) = -1.8\text{ V}\ (\text{at } I_D = I_{DSS}/2)$$

The resulting solution is:

$$V_{GS_Q} \cong \mathbf{-2.6\text{ V}}$$

b. From Fig. 7.28,

$$I_{D_Q} \cong \mathbf{3.8\text{ mA}}$$

c. $V_D = V_{DD} - I_D R_D$
$= 12\text{ V} - (3.8\text{ mA})(1.5\text{ k}\Omega) = 12\text{ V} - 5.7\text{ V}$
$= \mathbf{6.3\text{ V}}$

d. $V_G = \mathbf{0\text{ V}}$

e. $V_S = I_D R_S = (3.8\text{ mA})(680\ \Omega)$
$= \mathbf{2.58\text{ V}}$

f. $V_{DS} = V_D - V_S$
$= 6.3\text{ V} - 2.58\text{ V}$
$= \mathbf{3.72\text{ V}}$

7.6 SPECIAL CASE: $V_{GS_Q} = 0$ V

A network of recurring practical value because of its relative simplicity is the configuration of Fig. 7.29. Note that direct connection of the gate and source terminals to ground resulting in $V_{GS} = 0$ V. It specifies that for any dc condition the gate to source voltage must be zero volts. This will result in a vertical load line at $V_{GS_Q} = 0$V as shown in Fig. 7.30.

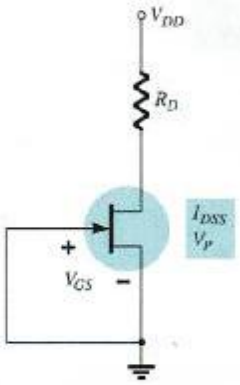


FIG. 7.29
Special case $V_{GS_Q} = 0$ V configuration.

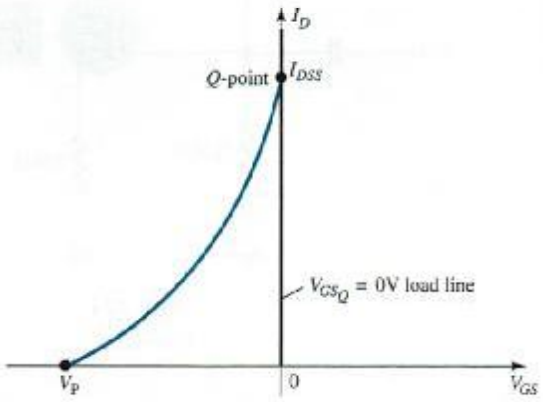


FIG. 7.30
Finding the Q-point for the network of Fig. 7.29.

Since the transfer curve of a JFET will cross the vertical axis at I_{DSS} the drain current for the network is set at that level.

Therefore,
$$I_{D_Q} = I_{DSS} \tag{7.29}$$

Applying Kirchhoff's voltage law:
$$V_{DD} - I_D R_D - V_{DS} = 0$$

and
$$V_{DS} = V_{DD} - I_D R_D \tag{7.30}$$

with
$$V_D = V_{DS} \tag{7.31}$$

and
$$V_S = 0\text{V} \tag{7.32}$$

7.7 DEPLETION-TYPE MOSFETs

The similarities in appearance between the transfer curves of JFETs and depletion-type MOSFETs permit a similar analysis of each in the dc domain. The primary difference between the two is the fact that depletion-type MOSFETs permit operating points with positive values of V_{GS} and levels of I_D that exceed I_{DSS}. In fact, for all the configurations discussed thus far, the analysis is the same if the JFET is replaced by a depletion-type MOSFET.

The only undefined part of the analysis is how to plot Shockley's equation for positive values of V_{GS}. How far into the region of positive values of V_{GS} and values of I_D greater than I_{DSS} does the transfer curve have to extend? For most situations, this required range will be fairly well defined by the MOSFET parameters and the resulting bias line of the network. A few examples will reveal the effect of the change in device on the resulting analysis.

EXAMPLE 7.7 For the *n*-channel depletion-type MOSFET of Fig. 7.31, determine:

a. I_{D_Q} and V_{GS_Q}.
b. V_{DS}.

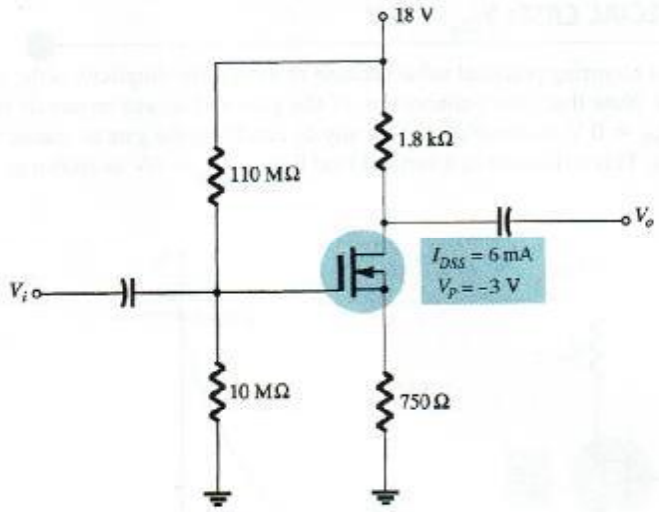


FIG. 7.31
Example 7.7.

Solution:

a. For the transfer characteristics, a plot point is defined by $I_D = I_{DSS}/4 = 6\text{ mA}/4 = 1.5\text{ mA}$ and $V_{GS} = V_P/2 = -3\text{ V}/2 = -1.5\text{ V}$. Considering the level of V_P and the fact that Shockley's equation defines a curve that rises more rapidly as V_{GS} becomes more positive, a plot point will be defined at $V_{GS} = +1\text{ V}$. Substituting into Shockley's equation yields

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2$$

$$= 6\text{ mA}\left(1 - \frac{+1\text{ V}}{-3\text{ V}}\right)^2 = 6\text{ mA}\left(1 + \frac{1}{3}\right)^2 = 6\text{ mA}(1.778)$$

$$= 10.67\text{ mA}$$

The resulting transfer curve appears in Fig. 7.32. Proceeding as described for JFETs, we have

$$\text{Eq. (7.15):} \quad V_G = \frac{10\text{ M}\Omega(18\text{ V})}{10\text{ M}\Omega + 110\text{ M}\Omega} = 1.5\text{ V}$$

$$\text{Eq. (7.16):} \quad V_{GS} = V_G - I_D R_S = 1.5\text{ V} - I_D(750\ \Omega)$$

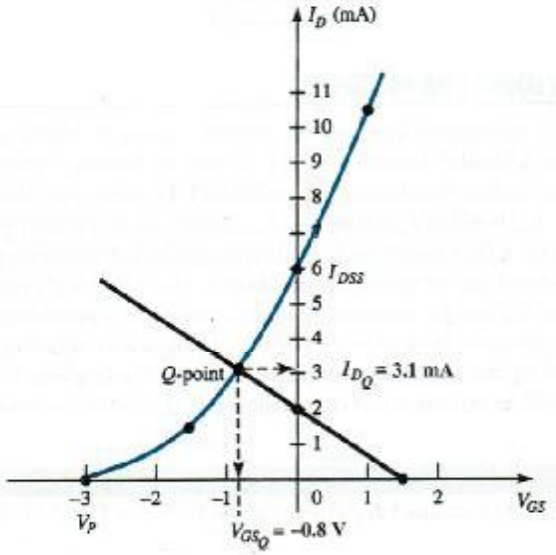


FIG. 7.32
Determining the Q-point for the network of Fig. 7.31.

Setting $I_D = 0$ mA results in

$$V_{GS} = V_G = 1.5\text{ V}$$

Setting $V_{GS} = 0$ V yields

$$I_D = \frac{V_G}{R_S} = \frac{1.5\text{ V}}{750\ \Omega} = 2\text{ mA}$$

The plot points and resulting bias line appear in Fig. 7.32. The resulting operating point is given by

$$I_{D_Q} = \mathbf{3.1\text{ mA}}$$
$$V_{GS_Q} = \mathbf{-0.8\text{ V}}$$

b. Eq. (7.19):

$$V_{DS} = V_{DD} - I_D(R_D + R_S)$$
$$= 18\text{ V} - (3.1\text{ mA})(1.8\text{ k}\Omega + 750\ \Omega)$$
$$\cong \mathbf{10.1\text{ V}}$$

EXAMPLE 7.8 Repeat Example 7.7 with $R_S = 150\ \Omega$.

Solution:

a. The plot points are the same for the transfer curve as shown in Fig. 7.33. For the bias line,

$$V_{GS} = V_G - I_D R_S = 1.5\text{ V} - I_D(150\ \Omega)$$

Setting $I_D = 0$ mA results in

$$V_{GS} = 1.5\text{ V}$$

Setting $V_{GS} = 0$ V yields

$$I_D = \frac{V_G}{R_S} = \frac{1.5\text{ V}}{150\ \Omega} = 10\text{ mA}$$

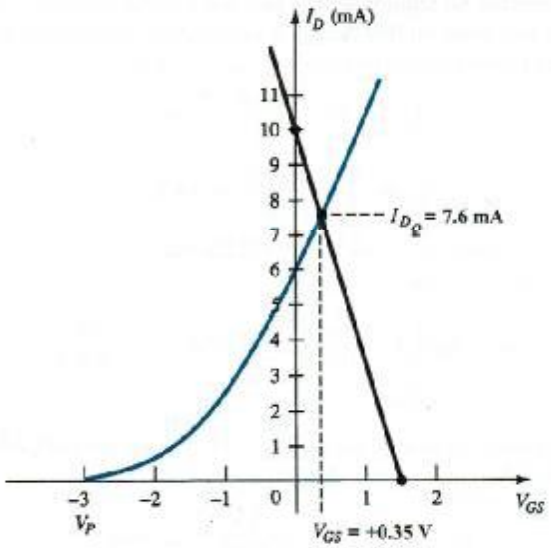


FIG. 7.33
Example 7.8.

The bias line is included on Fig. 7.33. Note in this case that the quiescent point results in a drain current that exceeds I_{DSS}, with a positive value for V_{GS}. The result is

$$I_{D_Q} = \mathbf{7.6\text{ mA}}$$
$$V_{GS_Q} = \mathbf{+0.35\text{ V}}$$

b. Eq. (7.19):

$$V_{DS} = V_{DD} - I_D(R_D + R_S)$$
$$= 18\text{ V} - (7.6\text{ mA})(1.8\text{ k}\Omega + 150\ \Omega)$$
$$= \mathbf{3.18\text{ V}}$$

EXAMPLE 7.9 Determine the following for the network of Fig. 7.34:

a. I_{D_Q} and V_{GS_Q}.
b. V_D.

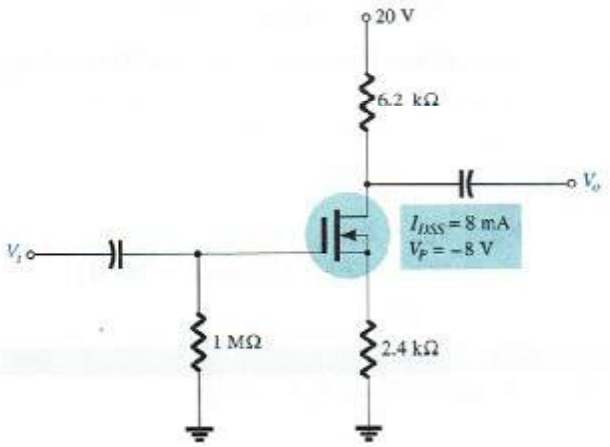


FIG. 7.34
Example 7.9.

Solution:

a. The self-bias configuration results in

$$V_{GS} = -I_D R_S$$

as obtained for the JFET configuration, establishing the fact that V_{GS} must be less than 0 V. There is therefore no requirement to plot the transfer curve for positive values of V_{GS}, although it was done on this occasion to complete the transfer characteristics. A plot point for the transfer characteristics for $V_{GS} < 0$ V is

$$I_D = \frac{I_{DSS}}{4} = \frac{8\text{ mA}}{4} = 2\text{ mA}$$

and

$$V_{GS} = \frac{V_P}{2} = \frac{-8\text{ V}}{2} = -4\text{ V}$$

and for $V_{GS} > 0$ V, since $V_P = -8$ V, we will choose

$$V_{GS} = +2\text{ V}$$

and

$$I_D = I_{DSS}\left(1 - \frac{V_{GS}}{V_P}\right)^2 = 8\text{ mA}\left(1 - \frac{+2\text{ V}}{-8\text{ V}}\right)^2$$

$$= 12.5\text{ mA}$$

The resulting transfer curve appears in Fig. 7.35. For the network bias line, at $V_{GS} = 0$ V, $I_D = 0$ mA. Choosing $V_{GS} = -6$ V gives

$$I_D = -\frac{V_{GS}}{R_S} = -\frac{-6\text{ V}}{2.4\text{ k}\Omega} = 2.5\text{ mA}$$

The resulting Q-point is given by

$$I_{D_Q} = \mathbf{1.7\text{ mA}}$$
$$V_{GS_Q} = \mathbf{-4.3\text{ V}}$$

b. $V_D = V_{DD} - I_D R_D$

$$= 20\text{ V} - (1.7\text{ mA})(6.2\text{ k}\Omega)$$

$$= \mathbf{9.46\text{ V}}$$

The example to follow employs a design that can also be applied to JFET transistors. At first impression it appears rather simplistic, but in fact it often causes some confusion when first analyzed due to the special point of operation.

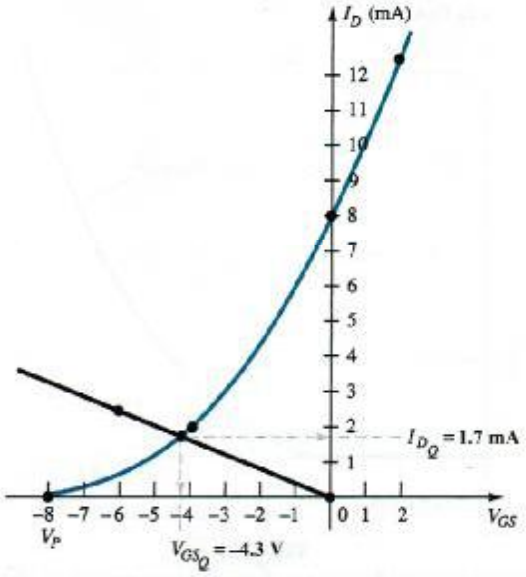


FIG. 7.35
Determining the Q-point for the network of Fig. 7.34.

EXAMPLE 7.10 Determine V_{DS} for the network of Fig. 7.36.

Solution: The direct connection between the gate and source terminals requires that

$$V_{GS} = 0\text{ V}$$

Since V_{GS} is fixed at 0 V, the drain current must be I_{DSS} (by definition). In other words,

$$V_{GS_Q} = \mathbf{0\text{ V}}$$

and

$$I_{D_Q} = \mathbf{10\text{ mA}}$$

There is therefore no need to draw the transfer curve, and

$$V_D = V_{DD} - I_D R_D = 20\text{ V} - (10\text{ mA})(1.5\text{ k}\Omega)$$
$$= 20\text{ V} - 15\text{ V}$$
$$= \mathbf{5\text{ V}}$$

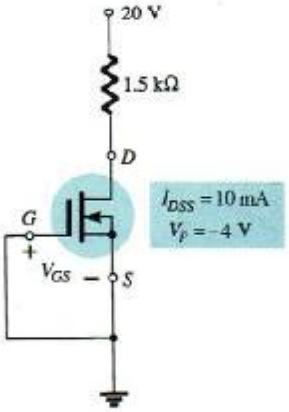


FIG. 7.36
Example 7.10.

7.8 ENHANCEMENT-TYPE MOSFETs

The transfer characteristics of the enhancement-type MOSFET are quite different from those encountered for the JFET and depletion-type MOSFETs, resulting in a graphical solution quite different from those of the preceding sections. First and foremost, recall that for the *n*-channel enhancement-type MOSFET, the drain current is zero for levels of gate-to-source voltage less than the threshold level $V_{GS(Th)}$, as shown in Fig. 7.37. For levels of V_{GS} greater than $V_{GS(Th)}$, the drain current is defined by

$$I_D = k(V_{GS} - V_{GS(Th)})^2 \qquad \textbf{(7.33)}$$

Since specification sheets typically provide the threshold voltage and a level of drain current ($I_{D(on)}$) and its corresponding level of $V_{GS(on)}$, two points are defined immediately as shown in Fig. 7.37. To complete the curve, the constant k of Eq. (7.33) must be determined from the specification sheet data by substituting into Eq. (7.33) and solving for k as follows:

$$I_D = k(V_{GS} - V_{GS(Th)})^2$$
$$I_{D(on)} = k(V_{GS(on)} - V_{GS(Th)})^2$$

which becomes the following after substituting Eq. (7.27):

$$V_{GS} = V_{DD} - I_D R_D \tag{7.36}$$

The result is an equation that relates the same two variables as Eq. (7.33), permitting the plot of both on the same set of axes.

Since Eq. (7.36) is that of a straight line, the same procedure described earlier can be employed to determine the two points that will define the plot on the graph. Substituting $I_D = 0$ mA into Eq. (7.36) gives

$$V_{GS} = V_{DD}|_{I_D = 0\text{ mA}} \tag{7.37}$$

Substituting $V_{GS} = 0$ V into Eq. (7.36), we have

$$I_D = \frac{V_{DD}}{R_D}\bigg|_{V_{GS} = 0\text{ V}} \tag{7.38}$$

The plots defined by Eqs. (7.33) and (7.36) appear in Fig. 7.40 with the resulting operating point.

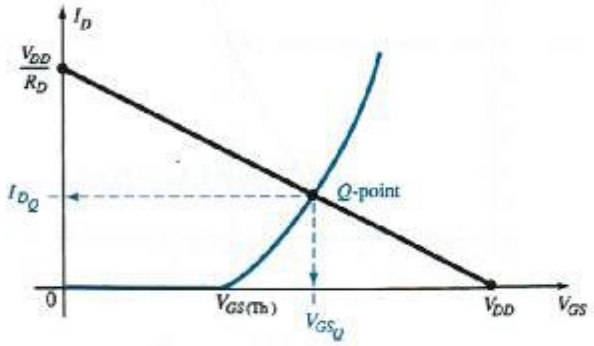


FIG. 7.40
Determining the Q-point for the network of Fig. 7.38.

EXAMPLE 7.11 Determine I_{D_Q} and V_{DS_Q} for the enhancement-type MOSFET of Fig. 7.41.

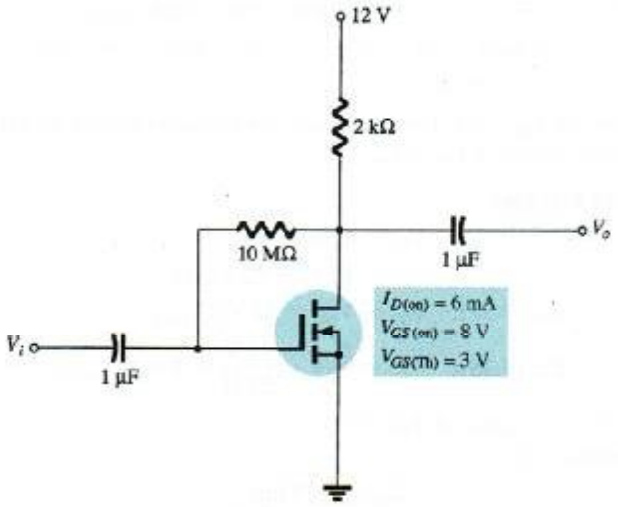


FIG. 7.41
Example 7.11.

Solution:

Plotting the Transfer Curve Two points are defined immediately as shown in Fig. 7.42. Solving for k, we obtain

$$\text{Eq. (7.34):} \quad k = \frac{I_{D(on)}}{(V_{GS(on)} - V_{GS(Th)})^2}$$

$$= \frac{6\text{ mA}}{(8\text{ V} - 3\text{ V})^2} = \frac{6 \times 10^{-3}}{25}\text{ A/V}^2$$

$$= \mathbf{0.24 \times 10^{-3}\ A/V^2}$$

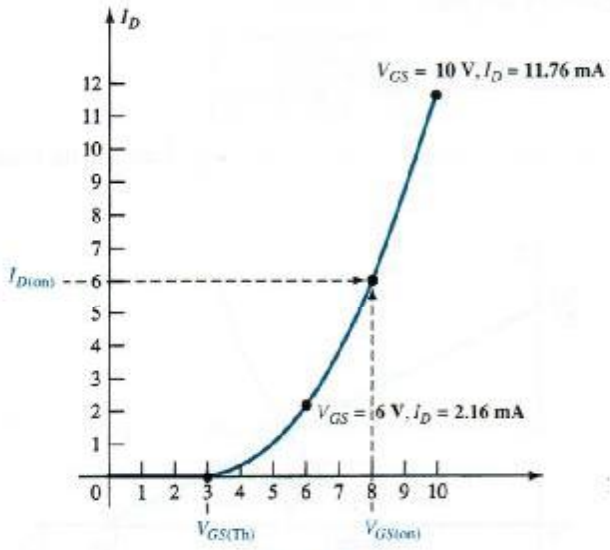


FIG. 7.42
Plotting the transfer curve for the MOSFET of Fig. 7.41.

For $V_{GS} = 6$ V (between 3 and 8 V):

$$I_D = 0.24 \times 10^{-3}(6\text{ V} - 3\text{ V})^2 = 0.24 \times 10^{-3}(9)$$

$$= 2.16\text{ mA}$$

as shown on Fig. 7.42. For $V_{GS} = 10$ V (slightly greater than $V_{GS(Th)}$),

$$I_D = 0.24 \times 10^{-3}(10\text{ V} - 3\text{ V})^2 = 0.24 \times 10^{-3}(49)$$

$$= 11.76\text{ mA}$$

as also appearing on Fig. 7.42. The four points are sufficient to plot the full curve for the range of interest as shown in Fig. 7.42.

For the Network Bias Line

$$V_{GS} = V_{DD} - I_D R_D$$

$$= 12\text{ V} - I_D(2\text{ k}\Omega)$$

$$\text{Eq. (7.37):} \quad V_{GS} = V_{DD} = 12\text{ V}|_{I_D = 0\text{ mA}}$$

$$\text{Eq. (7.38):} \quad I_D = \frac{V_{DD}}{R_D} = \frac{12\text{ V}}{2\text{ k}\Omega} = 6\text{ mA}|_{V_{GS} = 0\text{ V}}$$

The resulting bias line appears in Fig. 7.43.

At the operating point,

$$I_{D_Q} = \mathbf{2.75\text{ mA}}$$

and

$$V_{GS_Q} = 6.4\text{ V}$$

with

$$V_{DS_Q} = V_{GS_Q} = \mathbf{6.4\text{ V}}$$

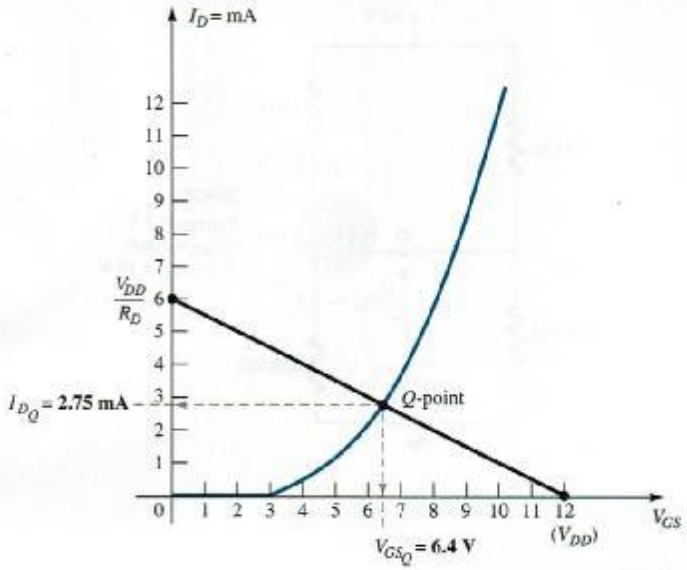


FIG. 7.43
Determining the Q-point for the network of Fig. 7.41.

Voltage-Divider Biasing Arrangement

A second popular biasing arrangement for the enhancement-type MOSFET appears in Fig. 7.44. The fact that $I_G = 0$ mA results in the following equation for V_{GG} as derived from an application of the voltage-divider rule:

$$V_G = \frac{R_2 V_{DD}}{R_1 + R_2} \tag{7.39}$$

Applying Kirchhoff's voltage law around the indicated loop of Fig. 7.43 results in

$$+V_G - V_{GS} - V_{R_S} = 0$$

and

$$V_{GS} = V_G - V_{R_S}$$

or

$$V_{GS} = V_G - I_D R_S \tag{7.40}$$

For the output section,

$$V_{R_S} + V_{DS} + V_{R_D} - V_{DD} = 0$$

and

$$V_{DS} = V_{DD} - V_{R_S} - V_{R_D}$$

or

$$V_{DS} = V_{DD} - I_D(R_S + R_D) \tag{7.41}$$

Since the characteristics are a plot of I_D versus V_{GS} and Eq. (7.40) relates the same two variables, the two curves can be plotted on the same graph and a solution determined at their intersection. Once I_{D_Q} and V_{GS_Q} are known, all the remaining quantities of the network such as V_{DS}, V_D, and V_S can be determined.

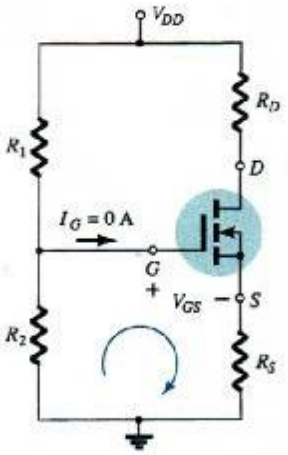


FIG. 7.44
Voltage-divider biasing arrangement for an n-channel enhancement MOSFET.

EXAMPLE 7.12 Determine I_{D_Q}, V_{GS_Q}, and V_{DS} for the network of Fig. 7.45.

Solution:

Network

$$\text{Eq. (7.39):} \quad V_G = \frac{R_2 V_{DD}}{R_1 + R_2} = \frac{(18\,\text{M}\Omega)(40\,\text{V})}{22\,\text{M}\Omega + 18\,\text{M}\Omega} = 18\,\text{V}$$

$$\text{Eq. (7.40):} \quad V_{GS} = V_G - I_D R_S = 18\,\text{V} - I_D(0.82\,\text{k}\Omega)$$

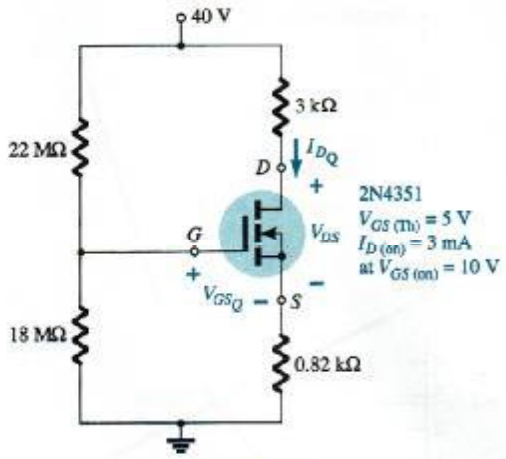


FIG. 7.45
Example 7.12.

When $I_D = 0$ mA,

$$V_{GS} = 18\text{ V} - (0\text{ mA})(0.82\text{ k}\Omega) = 18\text{ V}$$

as appearing on Fig. 7.46. When $V_{GS} = 0$ V,

$$V_{GS} = 18\text{ V} - I_D(0.82\text{ k}\Omega)$$
$$0 = 18\text{ V} - I_D(0.82\text{ k}\Omega)$$
$$I_D = \frac{18\text{ V}}{0.82\text{ k}\Omega} = 21.95\text{ mA}$$

as appearing on Fig. 7.46.

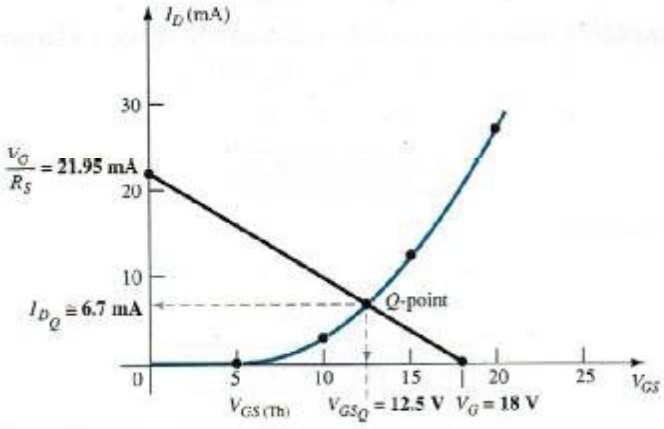


FIG. 7.46
Determining the Q-point for the network of Example 7.12.

Device

$$V_{GS(Th)} = 5\text{ V}, \qquad I_{D(on)} = 3\text{ mA with } V_{GS(on)} = 10\text{ V}$$

Eq. (7.34): $$k = \frac{I_{D(on)}}{(V_{GS(on)} - V_{GS(Th)})^2}$$
$$= \frac{3\text{ mA}}{(10\text{ V} - 5\text{ V})^2} = 0.12 \times 10^{-3}\text{ A/V}^2$$

and $$I_D = k(V_{GS} - V_{GS(Th)})^2$$
$$= 0.12 \times 10^{-3}(V_{GS} - 5)^2$$

which is plotted on the same graph (Fig. 7.46). From Fig. 7.46,

$$I_{D_Q} \cong \mathbf{6.7\ mA}$$
$$V_{GS_Q} = \mathbf{12.5\ V}$$

Eq. (7.41): $V_{DS} = V_{DD} - I_D(R_S + R_D)$
$$= 40\ \text{V} - (6.7\ \text{mA})(0.82\ \text{k}\Omega + 3.0\ \text{k}\Omega)$$
$$= 40\ \text{V} - 25.6\ \text{V}$$
$$= \mathbf{14.4\ V}$$

7.9 SUMMARY TABLE

Now that the most popular biasing arrangements for the various FETs have been introduced, Table 7.1 reviews the basic results and demonstrates the similarity in approach for a number of configurations. It also reveals that the general analysis of dc configurations for FETs is not overly complex. Once the transfer characteristics are established, the network self-bias line can be drawn and the Q-point determined at the intersection of the device transfer characteristic and the network bias curve. The remaining analysis is simply an application of the basic laws of circuit analysis.

7.10 COMBINATION NETWORKS

Now that the dc analysis of a variety of BJT and FET configurations is established, the opportunity to analyze networks with both types of devices presents itself. Fundamentally, the analysis simply requires that we *first* approach the device that will provide a terminal voltage or current level. The door is then usually open to calculating other quantities and concentrating on the remaining unknowns. These are usually particularly interesting problems due to the challenge of finding the opening and then using the results of the past few sections and Chapter 4 to find the important quantities for each device. The equations and relationships used are simply those we have employed on more than one occasion—there is no need to develop any new methods of analysis.

EXAMPLE 7.13 Determine the levels of V_D and V_C for the network of Fig. 7.47.

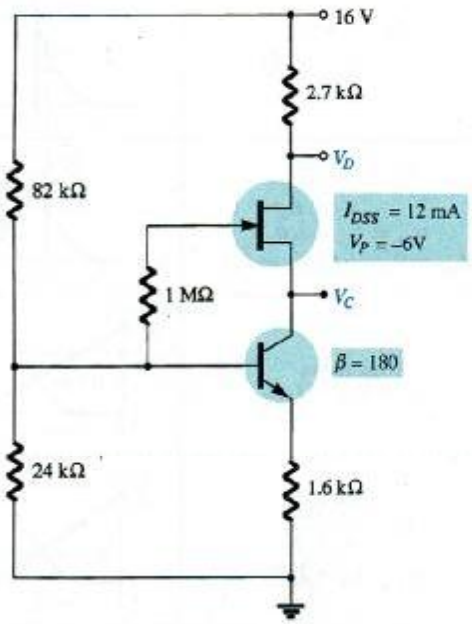


FIG. 7.47
Example 7.13.

Solution: From experience we now realize that V_{GS} is typically an important quantity to determine or write an equation for when analyzing JFET networks. Since V_{GS} is a level for which an immediate solution is not obvious, let us turn our attention to the transistor configuration. The voltage-divider configuration is one where the approximate technique can be applied ($\beta R_E = 180 \times 1.6\,\text{k}\Omega = 288\,\text{k}\Omega > 10R_2 = 240\,\text{k}\Omega$), permitting a determination of V_B using the voltage-divider rule on the input circuit.

For V_B,

$$V_B = \frac{24\,\text{k}\Omega(16\,\text{V})}{82\,\text{k}\Omega + 24\,\text{k}\Omega} = 3.62\,\text{V}$$

Using the fact that $V_{BE} = 0.7\,\text{V}$ results in

$$V_E = V_B - V_{BE} = 3.62\,\text{V} - 0.7\,\text{V} = 2.92\,\text{V}$$

and

$$I_E = \frac{V_{RE}}{R_E} = \frac{V_E}{R_E} = \frac{2.92\,\text{V}}{1.6\,\text{k}\Omega} = 1.825\,\text{mA}$$

with

$$I_C \cong I_E = 1.825\,\text{mA}$$

Continuing, we find for this configuration that

$$I_D = I_S = I_C$$

and

$$V_D = 16\,\text{V} - I_D(2.7\,\text{k}\Omega) = 16\,\text{V} - (1.825\,\text{mA})(2.7\,\text{k}\Omega) = 16\,\text{V} - 4.93\,\text{V} = \mathbf{11.07\,V}$$

The question of how to determine V_C is not as obvious. Both V_{CE} and V_{DS} are unknown quantities, preventing us from establishing a link between V_D and V_C or from V_E to V_D. A more careful examination of Fig. 7.47 reveals that V_C is linked to V_B by V_{GS} (assuming that $V_{R_G} = 0\,\text{V}$). Since we know V_B if we can find V_{GS}, V_C can be determined from

$$V_C = V_B - V_{GS}$$

The question then arises as to how to find the level of V_{GS_Q} from the quiescent value of I_D. The two are related by Shockley's equation:

$$I_{D_Q} = I_{DSS}\left(1 - \frac{V_{GS_Q}}{V_P}\right)^2$$

and V_{GS_Q} could be found mathematically by solving for V_{GS_Q} and substituting numerical values. However, let us turn to the graphical approach and simply work in the reverse order employed in the preceding sections. The JFET transfer characteristics are first sketched as shown in Fig. 7.48. The level of I_{D_Q} is then established by a horizontal line as shown in the same figure. V_{GS_Q} is then determined by dropping a line down from the operating point to the horizontal axis, resulting in

$$V_{GS_Q} = \mathbf{-3.7\,V}$$

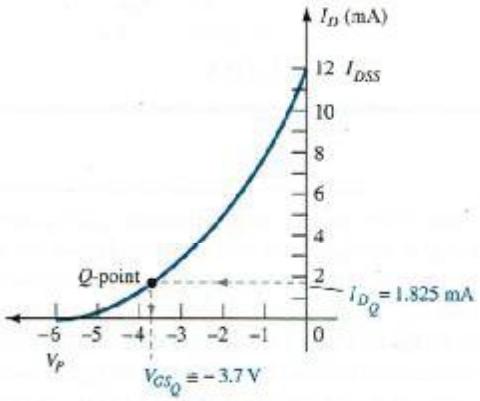


FIG. 7.48
Determining the Q-point for the network of Fig. 7.47.

The level of V_C is given by

$$V_C = V_B - V_{GS_Q} = 3.62\,\text{V} - (-3.7\,\text{V})$$
$$= \mathbf{7.32\,V}$$

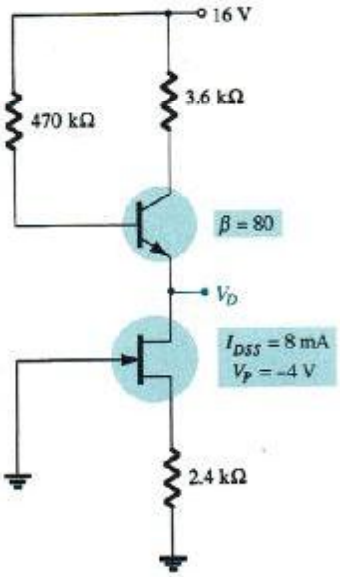


FIG. 7.49
Example 7.14.

EXAMPLE 7.14 Determine V_D for the network of Fig. 7.49.

Solution: In this case, there is no obvious path for determining a voltage or current level for the transistor configuration. However, turning to the self-biased JFET, we can derive an equation for V_{GS} and determine the resulting quiescent point using graphical techniques. That is,

$$V_{GS} = -I_D R_S = -I_D(2.4\,\text{k}\Omega)$$

resulting in the self-bias line appearing in Fig. 7.50, which establishes a quiescent point at

$$V_{GS_Q} = -2.6\,\text{V}$$
$$I_{D_Q} = 1\,\text{mA}$$

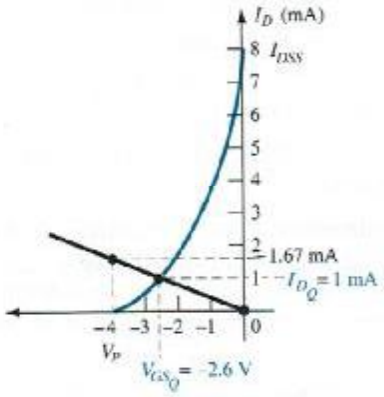


FIG. 7.50
Determining the Q-point for the network of Fig. 7.49.

For the transistor,

$$I_E \cong I_C = I_D = 1\,\text{mA}$$

and

$$I_B = \frac{I_C}{\beta} = \frac{1\,\text{mA}}{80} = 12.5\,\mu\text{A}$$

$$V_B = 16\,\text{V} - I_B(470\,\text{k}\Omega)$$
$$= 16\,\text{V} - (12.5\,\mu\text{A})(470\,\text{k}\Omega) = 16\,\text{V} - 5.875\,\text{V}$$
$$= 10.125\,\text{V}$$

and

$$V_E = V_D = V_B - V_{BE}$$
$$= 10.125\,\text{V} - 0.7\,\text{V}$$
$$= \mathbf{9.425\,V}$$

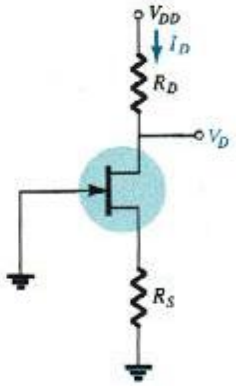


FIG. 7.51
Self-bias configuration to be designed.

7.11 DESIGN

The design process is not limited solely to dc conditions. The area of application, level of amplification desired, signal strength, and operating conditions are just a few of the conditions that enter into the total design process. However, we first concentrate on establishing the chosen dc conditions.

For example, if the levels of V_D and I_D are specified for the network of Fig. 7.51, the level of V_{GS_Q} can be determined from a plot of the transfer curve and R_S can then be determined from $V_{GS} = -I_D R_S$. If V_{DD} is specified, the level of R_D can then be calculated from $R_D = (V_{DD} - V_D)/I_D$. Of course, the values of R_S and R_D may not be standard commercial values, requiring that the nearest commercial values be employed. However, with the tolerance (range of values) normally specified for the parameters of a network, the slight

variation due to the choice of standard values will seldom cause a real concern in the design process.

The above is only one possibility for the design phase involving the network of Fig. 7.51. It is possible that only V_{DD} and R_D are specified together with the level of V_{DS}. The device to be employed may have to be specified along with the level of R_S. It appears logical that the device chosen should have a maximum V_{DS} greater than the specified value by a safe margin.

In general, it is good design practice for linear amplifiers to choose operating points that do not crowd the saturation level (I_{DSS}) or cutoff (V_P) regions. Levels of V_{GS_Q} close to $V_P/2$ or levels of I_{D_Q} near $I_{DSS}/2$ are certainly reasonable starting points in the design. Of course, in every design procedure the maximum levels of I_D and V_{DS} as appearing on the specification sheet must not be exceeded.

The examples to follow have a design or synthesis orientation in that specific levels are provided and network parameters such as R_D, R_S, V_{DD}, and so on, must be determined. In any case, the approach is in many ways the opposite of that described in previous sections. In some cases, it is just a matter of applying Ohm's law in its appropriate form. In particular, if resistive levels are requested, the result is often obtained simply by applying Ohm's law in the following form:

$$R_{\text{unknown}} = \frac{V_R}{I_R} \tag{7.42}$$

where V_R and I_R are often parameters that can be found directly from the specified voltage and current levels.

EXAMPLE 7.15 For the network of Fig. 7.52, the levels of V_{D_Q} and I_{D_Q} are specified. Determine the required values of R_D and R_S. What are the closest standard commercial values?

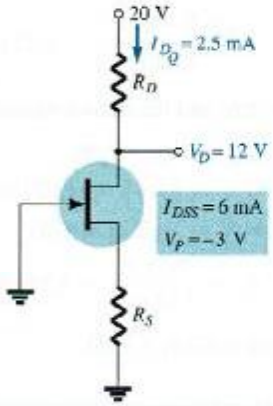


FIG. 7.52
Example 7.15.

Solution: As defined by Eq. (7.42),

$$R_D = \frac{V_{R_D}}{I_{D_Q}} = \frac{V_{DD} - V_{D_Q}}{I_{D_Q}}$$

and

$$= \frac{20\text{ V} - 12\text{ V}}{2.5\text{ mA}} = \frac{8\text{ V}}{2.5\text{ mA}} = \mathbf{3.2\,k\Omega}$$

Plotting the transfer curve in Fig. 7.53 and drawing a horizontal line at $I_{D_Q} = 2.5$ mA results in $V_{GS_Q} = -1$ V, and applying $V_{GS} = -I_D R_S$ establishes the level of R_S:

$$R_S = \frac{-(V_{GS_Q})}{I_{D_Q}} = \frac{-(-1\text{ V})}{2.5\text{ mA}} = \mathbf{0.4\,k\Omega}$$

The nearest standard commercial values are

$$R_D = 3.2\,\text{k}\Omega \Rightarrow \mathbf{3.3\,k\Omega}$$
$$R_S = 0.4\,\text{k}\Omega \Rightarrow \mathbf{0.39\,k\Omega}$$

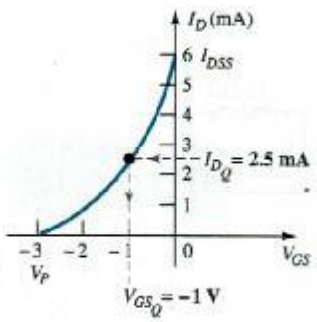


FIG. 7.53
Determining V_{GS_Q} for the network of Fig. 7.52.

EXAMPLE 7.16 For the voltage-divider bias configuration of Fig. 7.54, if $V_D = 12\text{ V}$ and $V_{GS_Q} = -2\text{ V}$, determine the value of R_S.

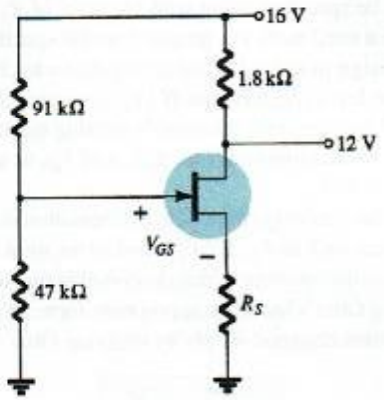


FIG. 7.54
Example 7.16.

Solution: The level of V_G is determined as follows:

$$V_G = \frac{47\text{ k}\Omega(16\text{ V})}{47\text{ k}\Omega + 91\text{ k}\Omega} = 5.44\text{ V}$$

with

$$I_D = \frac{V_{DD} - V_D}{R_D}$$

$$= \frac{16\text{ V} - 12\text{ V}}{1.8\text{ k}\Omega} = 2.22\text{ mA}$$

The equation for V_{GS} is then written and the known values substituted:

$$V_{GS} = V_G - I_D R_S$$

$$-2\text{ V} = 5.44\text{ V} - (2.22\text{ mA})R_S$$

$$-7.44\text{ V} = -(2.22\text{ mA})R_S$$

and

$$R_S = \frac{7.44\text{ V}}{2.22\text{ mA}} = \mathbf{3.35\text{ k}\Omega}$$

The nearest standard commercial value is 3.3 kΩ.

EXAMPLE 7.17 The levels of V_{DS} and I_D are specified as $V_{DS} = \frac{1}{2}V_{DD}$ and $I_D = I_{D(on)}$ for the network of Fig. 7.55. Determine the levels of V_{DD} and R_D.

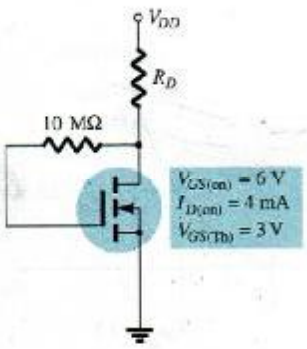


FIG. 7.55
Example 7.17.

Solution: Given $I_D = I_{D(on)} = 4\text{ mA}$ and $V_{GS} = V_{GS(on)} = 6\text{ V}$, for this configuration,

$$V_{DS} = V_{GS} = \tfrac{1}{2}V_{DD}$$

and

$$6\text{ V} = \tfrac{1}{2}V_{DD}$$

so that

$$V_{DD} = \mathbf{12\text{ V}}$$

Applying Eq. (7.42) yields

$$R_D = \frac{V_{R_D}}{I_D} = \frac{V_{DD} - V_{DS}}{I_{D(on)}} = \frac{V_{DD} - \frac{1}{2}V_{DD}}{I_{D(on)}} = \frac{\frac{1}{2}V_{DD}}{I_{D(on)}}$$

and

$$R_D = \frac{6\text{ V}}{4\text{ mA}} = \mathbf{1.5\text{ k}\Omega}$$

which is a standard commercial value.

ple will demonstrate that with the experience gained through the analysis of *n*-channel devices, the analysis of *p*-channel devices is quite straightforward.

EXAMPLE 7.18 Determine I_{D_Q}, V_{GS_Q}, and V_{DS} for the *p*-channel JFET of Fig. 7.58.

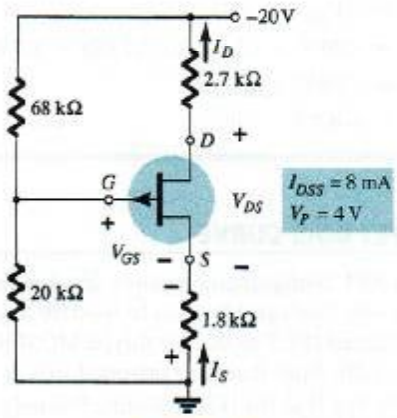


FIG. 7.58
Example 7.18.

Solution: We have

$$V_G = \frac{20\,\text{k}\Omega(-20\,\text{V})}{20\,\text{k}\Omega + 68\,\text{k}\Omega} = -4.55\,\text{V}$$

Applying Kirchhoff's voltage law gives

$$V_G - V_{GS} + I_D R_S = 0$$

and

$$V_{GS} = V_G + I_D R_S$$

Choosing $I_D = 0$ mA yields

$$V_{GS} = V_G = -4.55\,\text{V}$$

as appearing in Fig. 7.59.

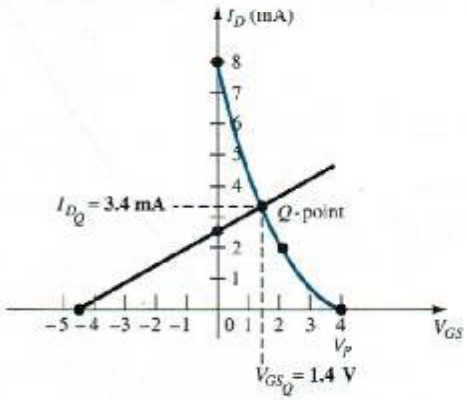


FIG. 7.59
Determining the Q-point for the JFET configuration of Fig. 7.58.

Choosing $V_{GS} = 0$ V, we obtain

$$I_D = -\frac{V_G}{R_S} = -\frac{-4.55\,\text{V}}{1.8\,\text{k}\Omega} = 2.53\,\text{mA}$$

as also appearing in Fig. 7.59.

The resulting quiescent point from Fig. 7.59 is given by

$$I_{D_Q} = \mathbf{3.4\ mA}$$
$$V_{GS_Q} = \mathbf{1.4\ V}$$

For V_{DS}, Kirchhoff's voltage law results in

$$-I_D R_S + V_{DS} - I_D R_D + V_{DD} = 0$$

and

$$\begin{aligned} V_{DS} &= -V_{DD} + I_D(R_D + R_S) \\ &= -20\ \text{V} + (3.4\ \text{mA})(2.7\ \text{k}\Omega + 1.8\ \text{k}\Omega) \\ &= -20\ \text{V} + 15.3\ \text{V} \\ &= \mathbf{-4.7\ V} \end{aligned}$$

7.14 UNIVERSAL JFET BIAS CURVE

Since the dc solution of a FET configuration requires drawing the transfer curve for each analysis, a universal curve was developed that can be used for any level of I_{DSS} and V_P. The universal curve for an *n*-channel JFET or depletion-type MOSFET (for negative values of V_{GS_Q}) is provided in Fig. 7.60. Note that the horizontal axis is not that of V_{GS} but of a normalized level defined by $V_{GS}/|V_P|$, the $|V_P|$ indicating that only the magnitude of V_P is to be employed, not its sign. For the vertical axis, the scale is also a normalized level of I_D/I_{DSS}. The result is that when $I_D = I_{DSS}$, the ratio is 1, and when $V_{GS} = V_P$, the ratio $V_{GS}/|V_P|$ is -1. Note also that the scale for I_D/I_{DSS} is on the left rather than on the right as encountered for I_D in past exercises. The additional two scales on the right need an introduction. The vertical scale labeled m can in itself be used to find the solution to fixed-bias configurations. The other scale, labeled M, is employed along with the m scale to find the solution to voltage-divider configurations. The scaling for m and M come from a mathematical development

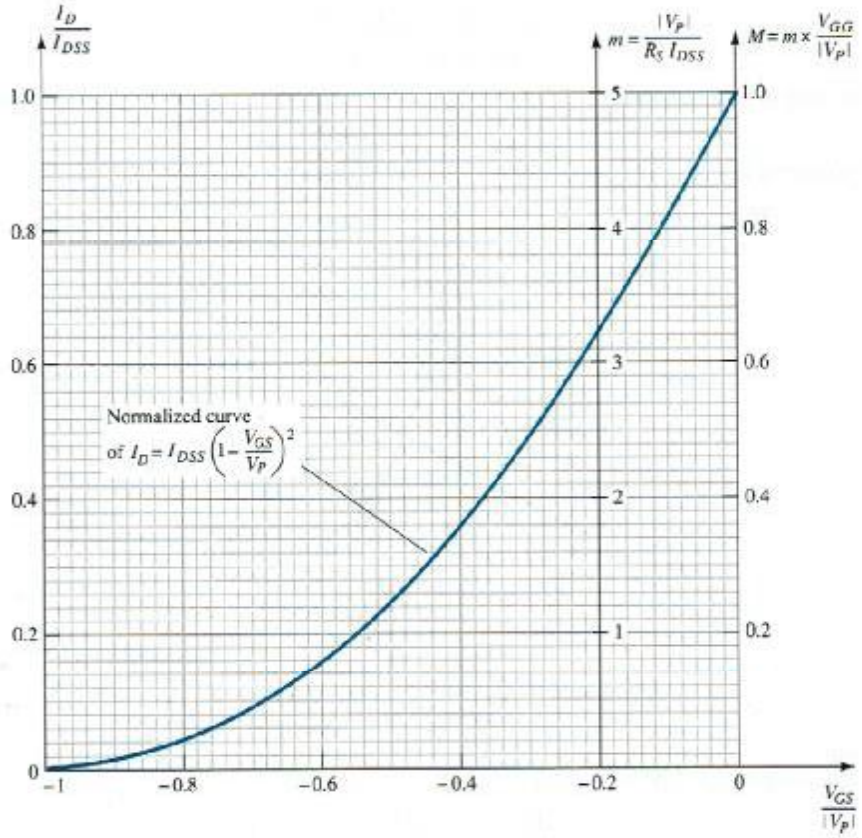


FIG. 7.60
Universal JFET bias curve.

PROBLEMS

Note: Asterisks indicate more difficult problems.

7.2 Fixed-Bias Configuration

1. For the fixed-bias configuration of Fig. 7.80:
   a. Sketch the transfer characteristics of the device.
   b. Superimpose the network equation on the same graph.
   c. Determine I_{D_Q} and V_{DS_Q}.
   d. Using Shockley's equation, solve for I_{D_Q} and then find V_{DS_Q}. Compare with the solutions of part (c).

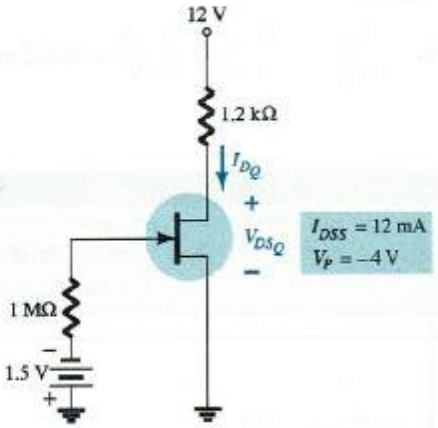


FIG. 7.80
Problems 1 and 35.

2. For the fixed-bias configuration of Fig. 7.81, determine:
   a. I_{D_Q} and V_{GS_Q} using a purely mathematical approach.
   b. Repeat part (a) using a graphical approach and compare results.
   c. Find V_{DS}, V_D, V_G, and V_S using the results of part (a).
3. Given the measured value of V_D in Fig. 7.82, determine:
   a. I_D.
   b. V_{DS}.
   c. V_{GG}.

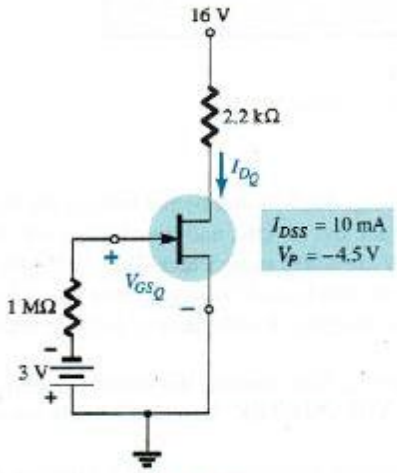


FIG. 7.81
Problem 2.

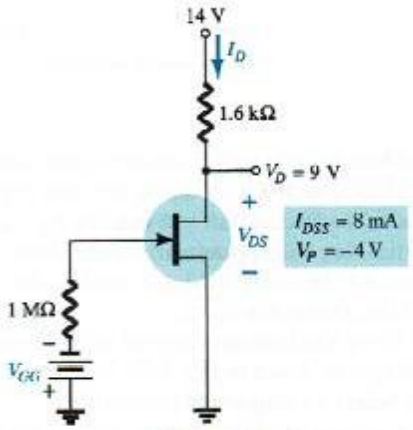


FIG. 7.82
Problem 3.

4. Determine V_D for the fixed-bias configuration of Fig. 7.83.
5. Determine V_D for the fixed-bias configuration of Fig. 7.84.

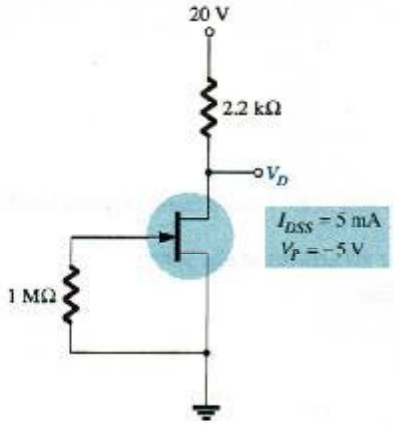


FIG. 7.83
Problem 4.

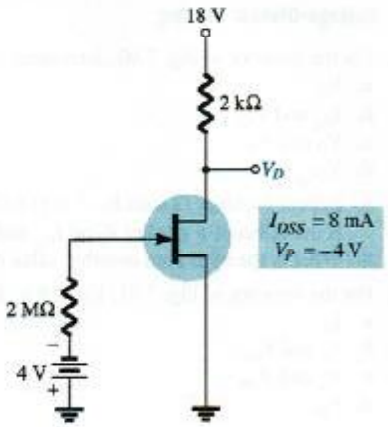


FIG. 7.84
Problem 5.

7.3 Self-Bias Configuration

6. For the self-bias configuration of Fig. 7.85:
   a. Sketch the transfer curve for the device.
   b. Superimpose the network equation on the same graph.
   c. Determine I_{D_Q} and V_{GS_Q}.
   d. Calculate V_{DS}, V_D, V_G, and V_S.

*7. Determine I_{D_Q} for the network of Fig. 7.84 using a purely mathematical approach. That is, establish a quadratic equation for I_D and choose the solution compatible with the network characteristics. Compare to the solution obtained in Problem 6.

8. For the network of Fig. 7.86, determine:
   a. V_{GS_Q} and I_{D_Q}.
   b. V_{DS}, V_D, V_G, and V_S.

9. Given the measurement $V_S = 1.7$ V for the network of Fig. 7.87, determine:
   a. I_{D_Q}.
   b. V_{GS_Q}.
   c. I_{DSS}.
   d. V_D.
   e. V_{DS}.

*10. For the network of Fig. 7.88, determine:
   a. I_D.
   b. V_{DS}.
   c. V_D.
   d. V_S.

*11. Find V_S for the network of Fig. 7.89.

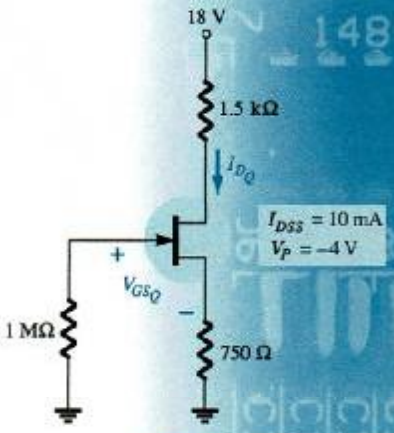


FIG. 7.85
Problems 6, 7, and 36.

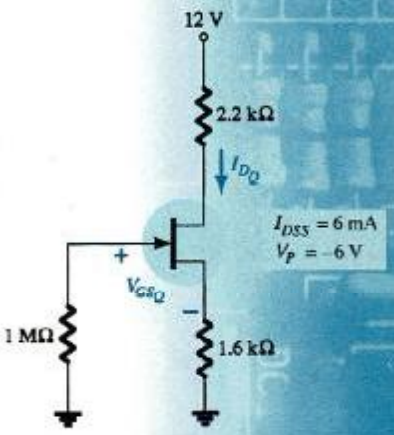


FIG. 7.86
Problem 8.

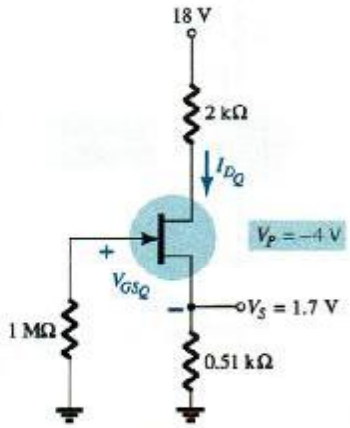


FIG. 7.87
Problem 9.

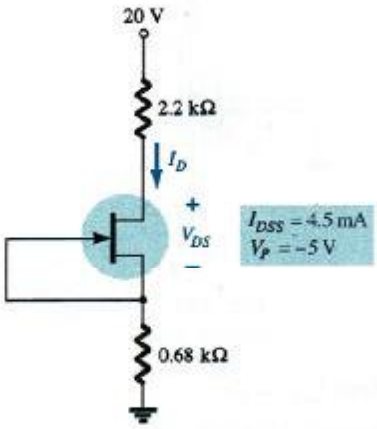


FIG. 7.88
Problem 10.

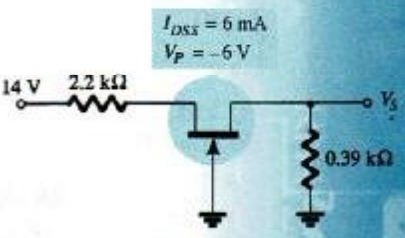


FIG. 7.89
Problem 11.

7.4 Voltage-Divider Biasing

12. For the network of Fig. 7.90, determine:
    a. V_G.
    b. I_{D_Q} and V_{GS_Q}.
    c. V_D and V_S.
    d. V_{DS_Q}.
13. a. Repeat Problem 12 with $R_S = 0.51\ \text{k}\Omega$ (about 50% of the value of that of Problem 12). What is the effect of a smaller R_S on I_{D_Q} and V_{GS_Q}?
    b. What is the minimum possible value of R_S for the network of Fig. 7.90?
14. For the network of Fig. 7.91, $V_D = 9\ \text{V}$. Determine:
    a. I_D.
    b. V_S and V_{DS}.
    c. V_G and V_{GS}.
    d. V_P.

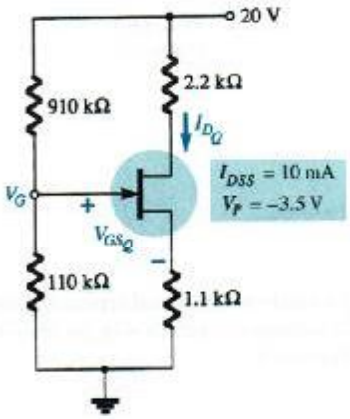


FIG. 7.90
Problems 12 and 13.

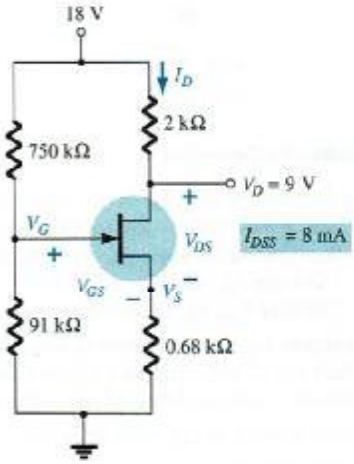


FIG. 7.91
Problem 14.

7.5 Common-Gate Configuration

*15. For the network of Fig. 7.92, determine:
    a. I_{D_Q} and V_{GS_Q}.
    b. V_{DS} and V_S.
*16. Given $V_{DS} = 4\ \text{V}$ for the network of Fig. 7.93, determine:
    a. I_D.
    b. V_D and V_S.
    c. V_{GS}.

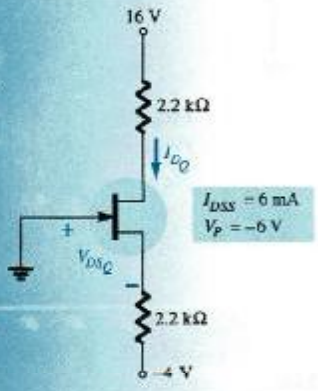


FIG. 7.92
Problems 15 and 37.

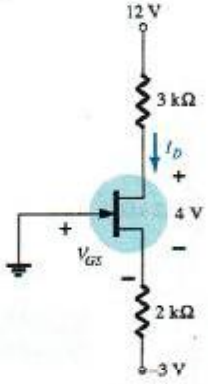


FIG. 7.93
Problem 16.

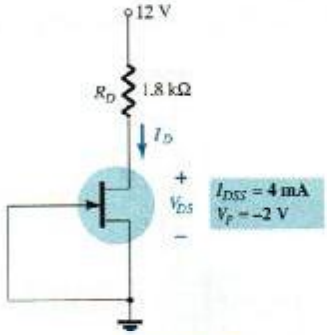


FIG. 7.94
Problems 17.

7.6 Special Case: $V_{GS_Q} = 0\text{V}$

17. For the network of Fig. 7.94.
    a. Find I_{D_Q}.
    b. Determine V_{D_Q} and V_{DS_Q}.
    c. Find the power supplied by the source and dissipated by the device.

7.7 Depletion-Type MOSFETs

18. For the self-bias configuration of Fig. 7.95, determine:
    a. I_{D_Q} and V_{GS_Q}.
    b. V_{DS} and V_D.

*19. For the network of Fig. 7.96, determine:
    a. I_{D_Q} and V_{GS_Q}.
    b. V_{DS} and V_S.

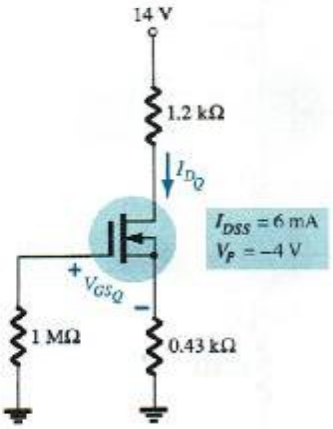


FIG. 7.95
Problem 18.

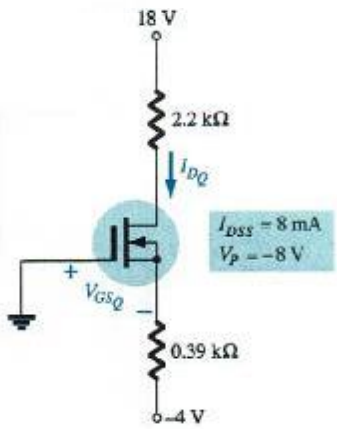


FIG. 7.96
Problem 19.

7.8 Enhancement-Type MOSFETs

20. For the network of Fig. 7.97, determine:
    a. I_{D_Q}.
    b. V_{GS_Q} and V_{DS_Q}.
    c. V_D and V_S.
    d. V_{DS}.

21. For the voltage-divider configuration of Fig. 7.98, determine:
    a. I_{D_Q} and V_{GS_Q}.
    b. V_D and V_S.

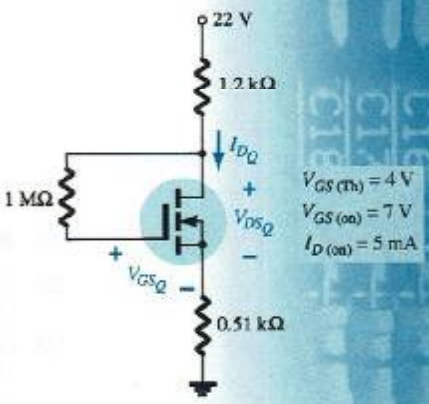


FIG. 7.97
Problem 20.

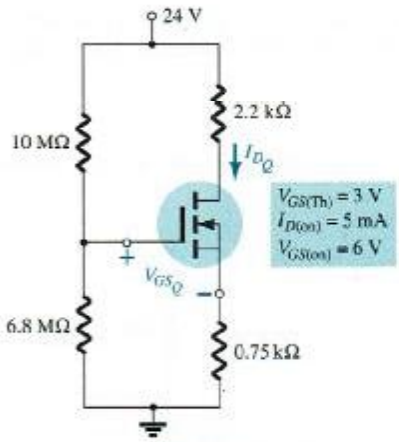


FIG. 7.98
Problem 21.

7.10 Combination Networks

*22. For the network of Fig. 7.99, determine:
    a. V_G.
    b. V_{GS_Q} and I_{D_Q}.
    c. I_E.
    d. I_B.
    e. V_D.
    f. V_C.

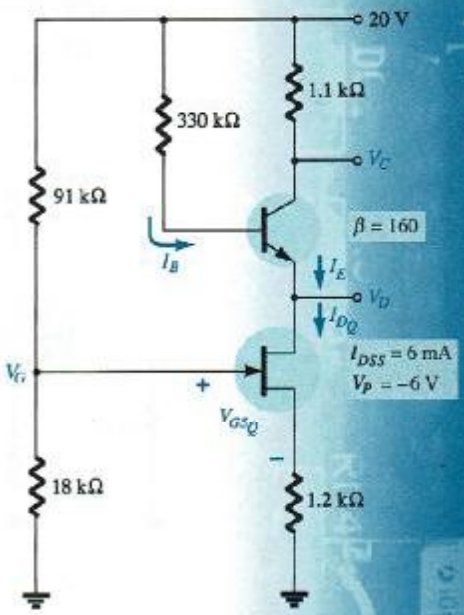


FIG. 7.99
Problem 22.

*23. For the combination network of Fig. 7.100, determine:
a. V_B and V_G.
b. V_E.
c. I_E, I_C, and I_D.
d. I_B.
e. V_C, V_S, and V_D.
f. V_{CE}.
g. V_{DS}.

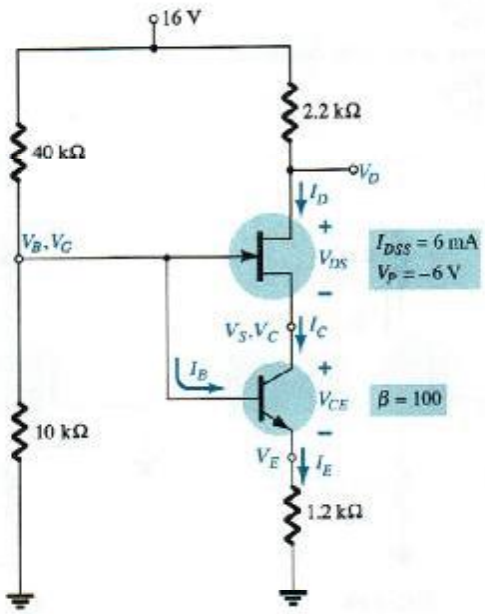


FIG. 7.100
Problem 23.

7.11 Design

*24. Design a self-bias network using a JFET transistor with $I_{DSS} = 8$ mA and $V_P = -6$ V to have a Q-point at $I_{D_Q} = 4$ mA using a supply of 14 V. Assume that $R_D = 3R_S$ and use standard values.

*25. Design a voltage-divider bias network using a depletion-type MOSFET with $I_{DSS} = 10$ mA and $V_P = -4$ V to have a Q-point at $I_{D_Q} = 2.5$ mA using a supply of 24 V. In addition, set $V_G = 4$ V and use $R_D = 2.5R_S$ with $R_1 = 22\,\text{M}\Omega$. Use standard values.

26. Design a network such as appears in Fig. 7.40 using an enhancement-type MOSFET with $V_{GS(Th)} = 4$ V and $k = 0.5 \times 10^{-3}\,\text{A/V}^2$ to have a Q-point of $I_{D_Q} = 6$ mA. Use a supply of 16 V and standard values.

7.12 Troubleshooting

*27. What do the readings for each configuration of Fig. 7.101 suggest about the operation of the network?

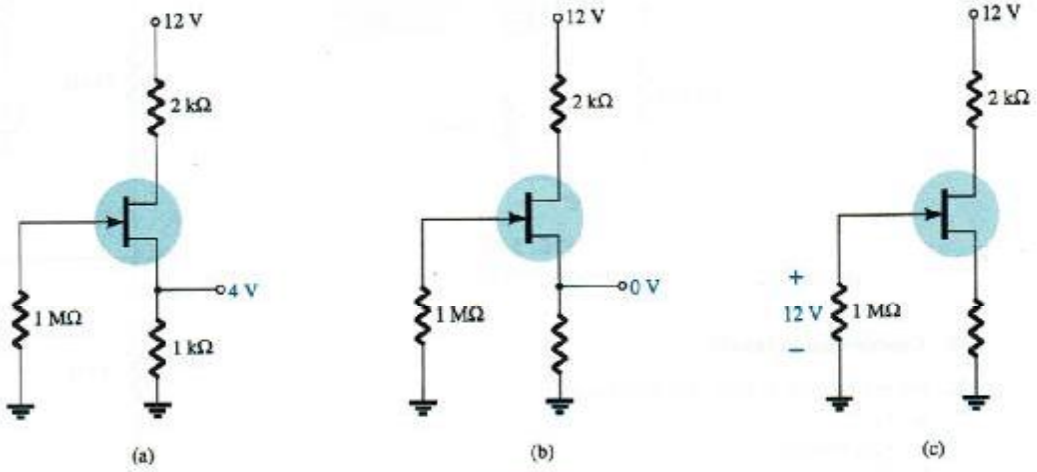


FIG. 7.101
Problem 27.

*28. Although the readings of Fig. 7.102 initially suggest that the network is behaving properly, determine a possible cause for the undesirable state of the network.

*29. The network of Fig. 7.103 is not operating properly. What is the specific cause for its failure?

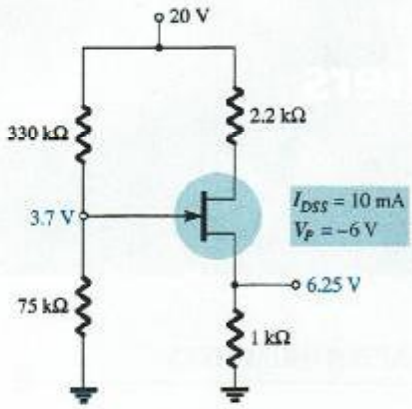


FIG. 7.102
Problem 28.

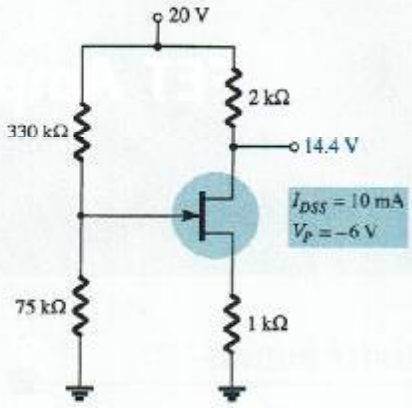


FIG. 7.103
Problem 29.

7.13 *p*-Channel FETs

30. For the network of Fig. 7.104, determine:
   a. I_{D_Q} and V_{GS_Q}.
   b. V_{DS}.
   c. V_D.

31. For the network of Fig. 7.105, determine:
   a. I_{D_Q} and V_{GS_Q}.
   b. V_{DS}.
   c. V_D.

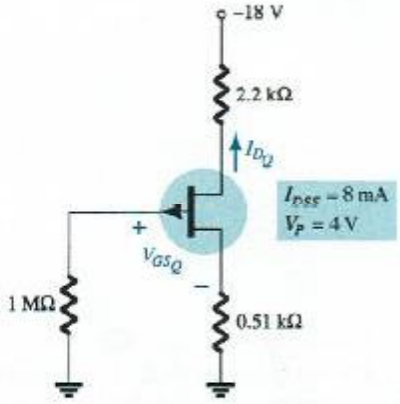


FIG. 7.104
Problem 30.

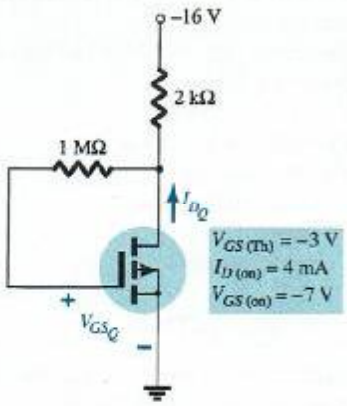


FIG. 7.105
Problem 31.

7.14 Universal JFET Bias Curve

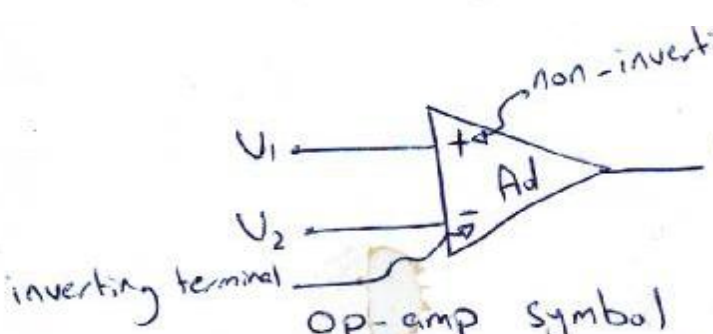
32. Repeat Problem 1 using the universal JFET bias curve.
33. Repeat Problem 6 using the universal JFET bias curve.
34. Repeat Problem 12 using the universal JFET bias curve.
35. Repeat Problem 15 using the universal JFET bias curve.

7.15 Computer Analysis

36. Perform a PSpice Windows analysis of the network of Problem 1.
37. Perform a PSpice Windows analysis of the network of Problem 6.
38. Perform a Multisim analysis of the network of Problem 15.
39. Perform a Multisim analysis of the network of Problem 31.

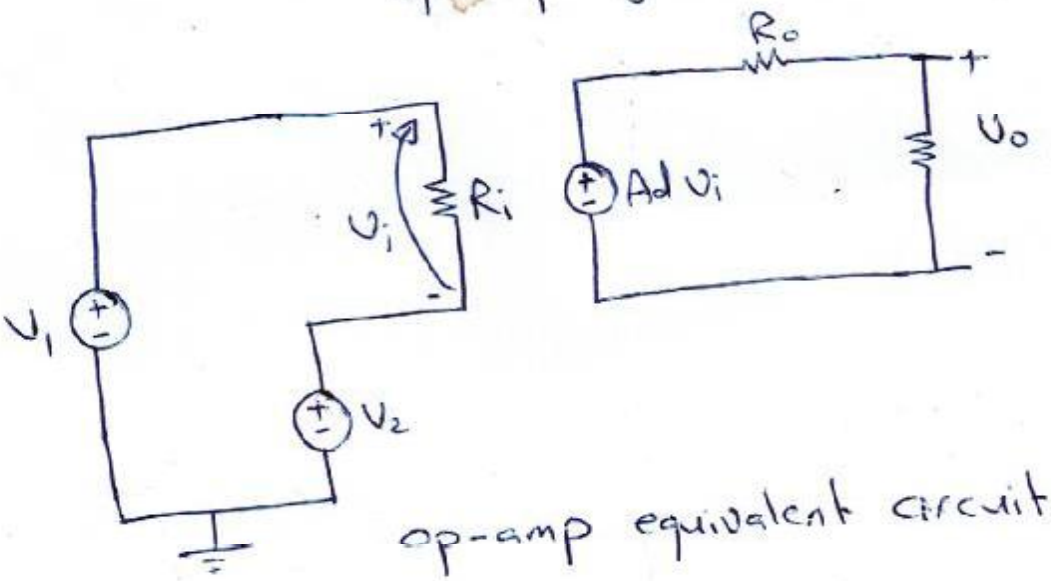
Operational Amplifier

An Operational amplifier (op-amp) is an integrated circuit that amplifies the difference between two input voltages and produces a single output.



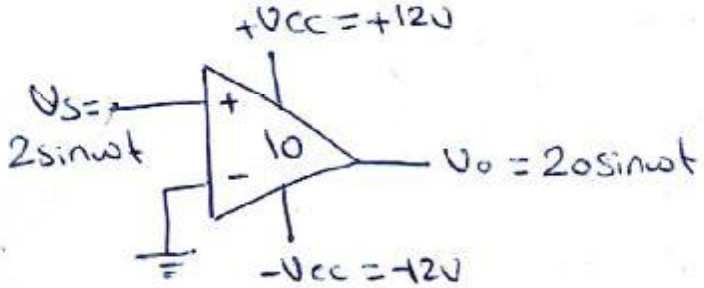
$V_o = (V_1 - V_2)\,Ad$
$= V_i\,Ad.$

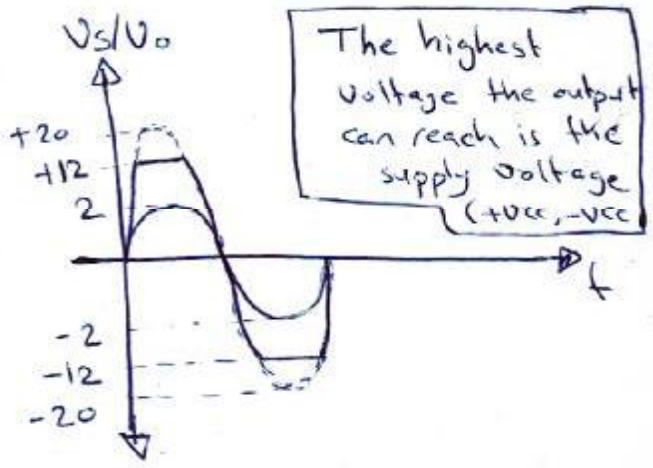
op-amp symbol



op-amp equivalent circuit.

The op-amp is used to perform a variety of functions (operations).





Ideal Operational Amplifier :-

The ideal op-amp has the following c/cs :-

1 - Input resistance $R_i \rightarrow \infty$.

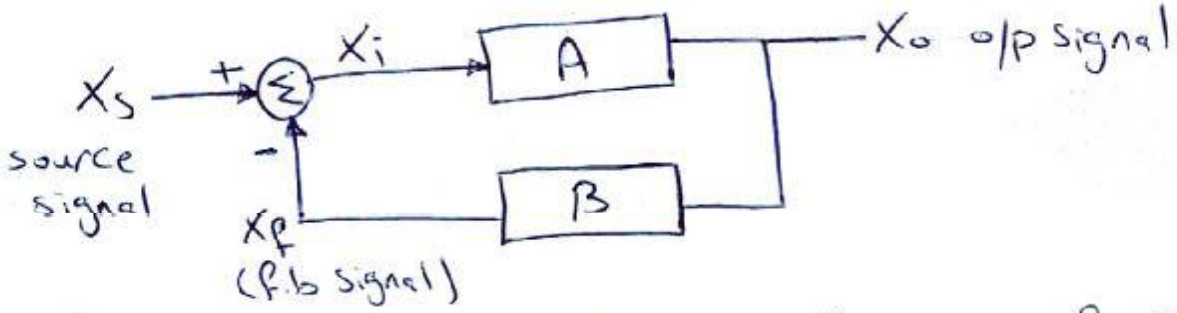
2 - Output resistance $R_o \rightarrow 0$.

3 - Voltage gain $A_d \rightarrow \infty$.

4 - Bandwidth $BW \rightarrow \infty$.

5 - when $V_1 = V_2$, $V_o = 0$ V.

$A_v \rightarrow \infty$ implies that $V_i = 0$, when the op-amp is used in linear applications. Such applications must employ negative feedback around the op-amp.



Block diagram of a -ve feedback system.

$$X_o = A X_i \quad \text{---} (1)$$

$$X_f = \beta X_o \quad \text{---} (2)$$

$$X_f + X_i = X_s \quad \text{---} (3)$$

Solving equations ①, ② and ③ for A_f where $A_f = \frac{X_o}{X_s}$:-

$$A_f = \frac{A}{1+\beta A}$$

A_f :- gain with feedback.

A :- gain without feedback.

$|A_f| < |A|$

$$A_{f\,max} = \lim_{A \to \infty} A_f = \lim_{A \to \infty} \frac{1}{\frac{1}{A} + \beta} = \frac{1}{\beta} \text{ (finite value)}$$

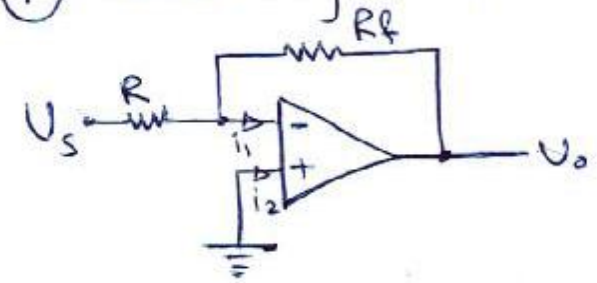
$\therefore X_o = A_f X_s$ is finite for a finite X_s.

$$\therefore X_i = \frac{X_o}{A} = \frac{X_o(\text{finite})}{\infty} = 0$$

$A_v \to \infty$ must imply $v_i = 0$ for an ideal op-amp. with -ve f.b. (linear applications).

Linear Applications

① Inverting Amplifier



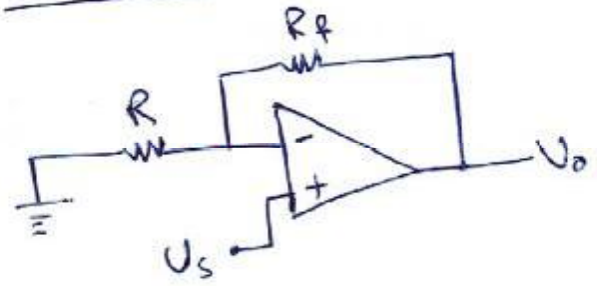
Since R_i (op-amp) $\to \infty$ $\therefore i_1 = 0$, $i_2 = 0$

and since $A_d \to \infty$ and (-ve f.b) then $v_i = 0$

$$\therefore \frac{V_s}{R} = \frac{-V_o}{R_f}$$

$$\frac{V_o}{V_s} = \frac{-R_f}{R} = A_{vf} = \text{voltage gain with f.b.}$$

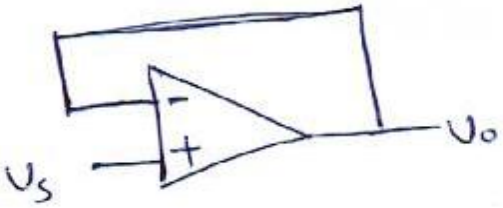
2) Non - Inverting Amplifier :-



$$V_s\left(\frac{1}{R} + \frac{1}{R_f}\right) = \frac{V_o}{R_f}$$

$$\frac{V_o}{V_s} = \left(1 + \frac{R_f}{R}\right) = A_{vf}.$$

if $R_f = 0$

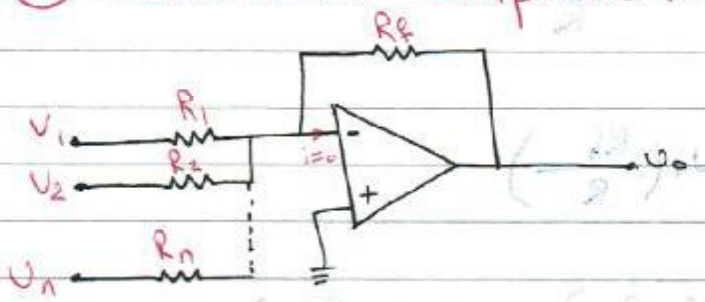


$$\frac{V_o}{V_s} = 1 \;,\; R_o = 0 \;,\; R_i = \infty$$

This is an op-amp as a buffer (voltage follower).

Subject : Date:

③ Summation Amplifier :-



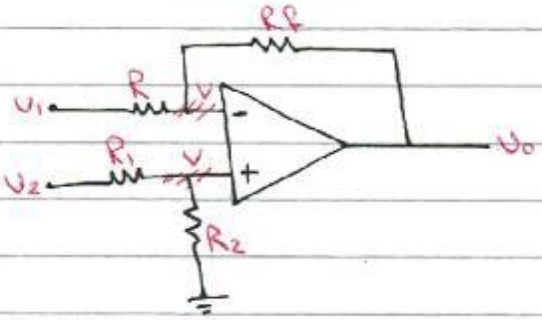
$$\frac{-V_o}{R_f} = \frac{V_1}{R_1} + \frac{V_2}{R_2} + \cdots + \frac{V_n}{R_n}$$

if $R_1 = R_2 = \cdots = R_n$

$$\frac{-V_o}{R_f} = \frac{1}{R_n}\left(V_1 + V_2 + \cdots + V_n\right)$$

$$V_o = \frac{-R_f}{R_n}\left(V_1 + V_2 + \cdots + V_n\right)$$

④ Difference Amplifier



$$V = V_2 \frac{R_2}{R_1 + R_2}$$

$$\frac{V_1 - V}{R} = \frac{V - V_o}{R_f} \Rightarrow \frac{V_1}{R} - \frac{V}{R} = \frac{V}{R_f} - \frac{V_o}{R_f}$$

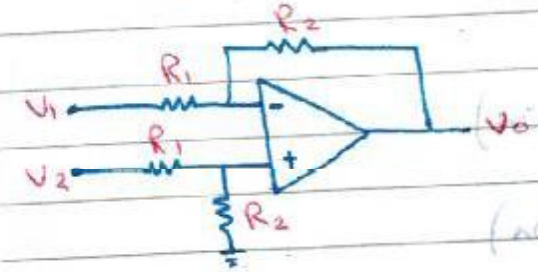
Subject : Date:

$$\frac{V_o}{R_f} = V\left(\frac{R_f + R}{R R_f}\right) - \frac{V_1}{R}$$

$$V_o = V\left(\frac{R_f + R}{R}\right) - V_1\left(\frac{R_f}{R}\right)$$

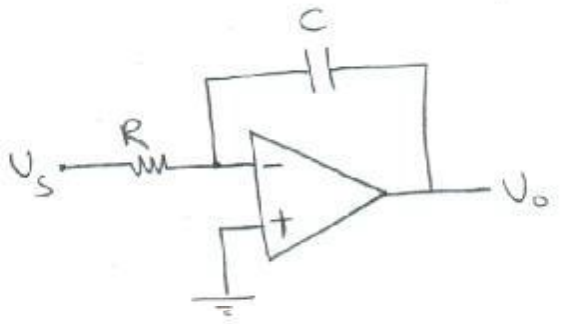
$$V_o = V_2\left(\frac{R_2}{R_1 + R_2}\right)\left(\frac{R_f + R}{R}\right) - V_1\left(\frac{R_f}{R_1}\right)$$

if $R_f = R_2$ and $R = R_1$



$$V_o = \frac{R_2}{R_1}(V_2 - V_1)$$

Miller Integrator:-



* At D.C ($\omega=0$) the capacitor behaves as an open cct., there is no negative feedback.

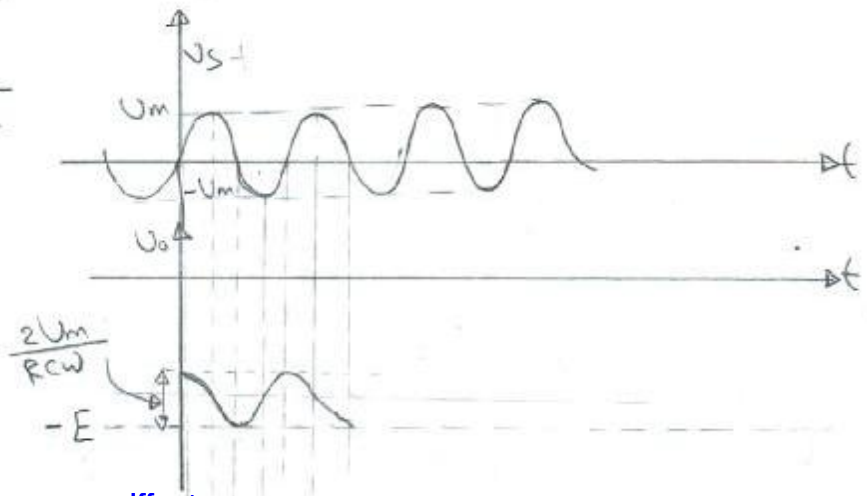
* This is very important in the integrator cct. and is a problem, because any tiny DC Component in the input signal will theoretically produce an infinite output. Ofcourse, no infinite o/p voltage results in practice, rather the o/p of the op-amp. Saturates at a voltage close to the op-amp. +ve or -ve power supply depending on the polarity of the input D.C signal.

$$\frac{V_o(j\omega)}{V_s(j\omega)} = \frac{-1}{j\omega RC}$$ (transfer c/c's of the Miller Integrator).

for example:-

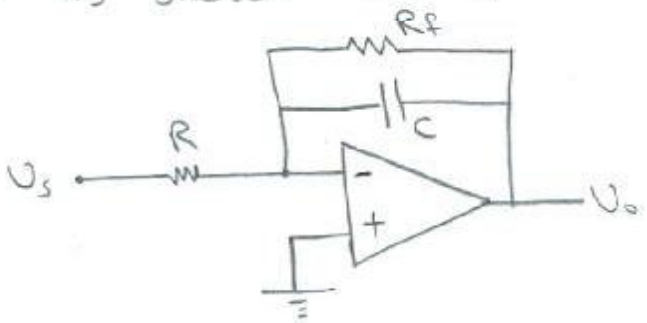
$V_s = V_m \sin\omega t + \epsilon$, $\epsilon \to 0$ (ϵ is +ve)

$$V_o = \frac{V_m}{RC\omega}\cos\omega t - \frac{\epsilon t}{RC}$$



E :- Saturation voltage of the op-amp

To avoid this problem a resistor is added in parallel with the capacitor. If $R_f \gg X_c$ the new circuit will be as close to the Miller Integrator as possible. The new circuit is called the D.C clamped integrator as shown below:-



$$\frac{V_o(j\omega)}{V_s(j\omega)} = \frac{-1}{\frac{R}{R_f} + j\omega RC}$$

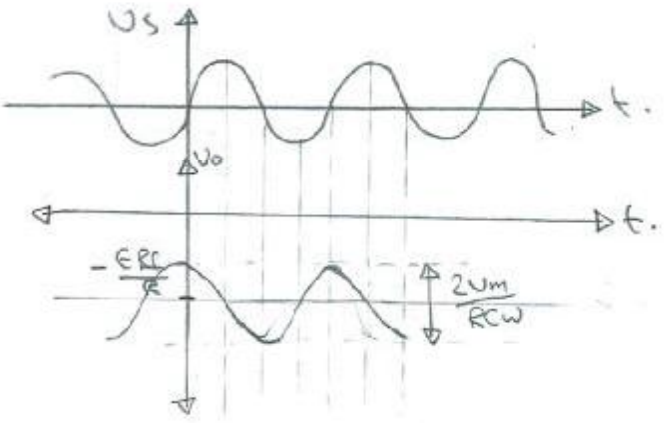
if $\omega = 0$ (D.C) then $\frac{V_o(j\omega)}{V_s(j\omega)} = -\frac{R_f}{R}$

if $\omega \neq 0$ the $\frac{V_o(j\omega)}{V_s(j\omega)} \approx \frac{-1}{j\omega RC}$ since $R_f \gg X_c$

for example:-

$V_s = \epsilon + V_m \sin\omega t$, $(\epsilon \to 0)$ ϵ is +ve

$V_o \approx -\epsilon \frac{R_f}{R} + \frac{V_m}{RC\omega} \cos\omega t$

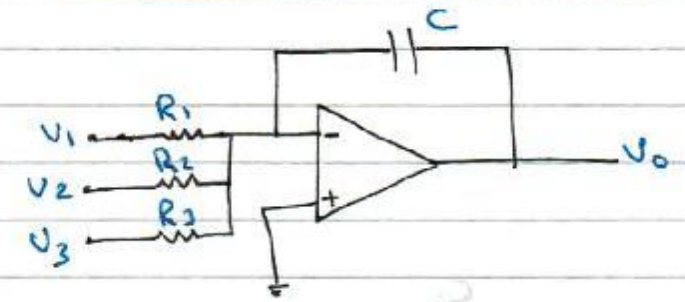


Analog Computer

One of the op-amp applications is an analog computer. The Analog Computer consists of a number of inverters, Summers, integrators and Summer-integrators that can be connected together to solve differential equations in real time.

Subject : Date:

⑥ The Summer integrator unit:-



$$\frac{V_1}{R_1} + \frac{V_2}{R_2} + \frac{V_3}{R_3} = -C\frac{dV_o}{dt}$$

$$V_o = -\int\left[\frac{V_1}{CR_1} + \frac{V_2}{CR_2} + \frac{V_3}{CR_3}\right]dt$$

Example:-

Solve the following differential equation using an analog computer :-

$$\frac{V_o}{3} + 2\frac{dV_o}{dt} + \frac{d^2V_o}{dt^2} = V_m \cos\omega t \quad , \quad \left.\frac{dV_o}{dt}\right|_{t=0} = -1V$$

Solution:-

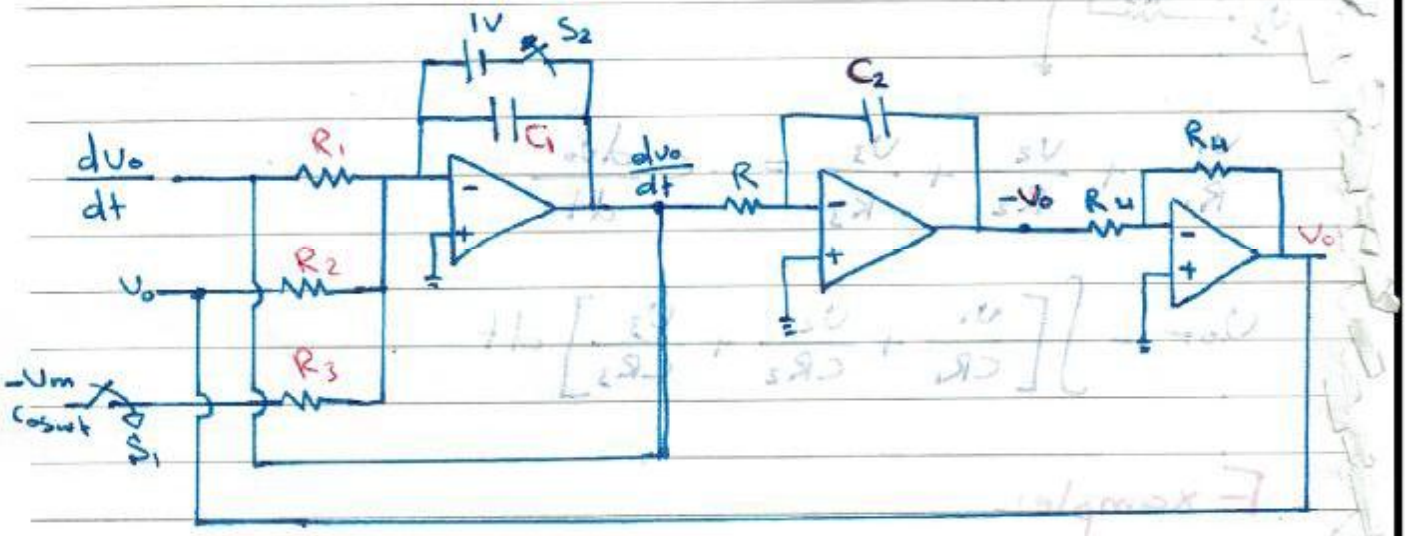
$$\frac{d^2V_o}{dt^2} = -2\frac{dV_o}{dt} - \frac{V_o}{3} + V_m \cos\omega t$$

$$\frac{dV_o}{dt} = \int_0^t \frac{d^2V_o}{d\lambda^2}\,d\lambda$$

Subject : Date:

$$\frac{dv_o}{dt} = \int_0^t \left(-2\frac{dv_o}{d\lambda} - \frac{v_o}{3} + v_m \cos\omega\lambda \right) d\lambda$$

$$v_o = \int_0^t \frac{dv_o}{d\lambda}\, d\lambda$$



Initially S_1 is opened and S_2 is closed, then close S_1 and open S_2 simultaneously to start operation.

$$\frac{1}{R_1 C_1} = 2$$

$$\frac{1}{R_2 C_1} = \frac{1}{3} \quad \text{if } C_1 = 1\mu F$$

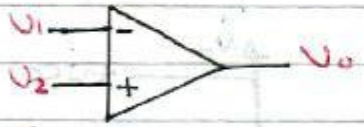
$$\frac{1}{R_3 C_1} = 1 \quad \therefore R_1 = 0.5\,M\Omega,\ R_2 = 3\,M\Omega,\ R_3 = 1\,M\Omega$$

$$\frac{1}{RC_2} = 1 \quad \text{if } C_2 = 1\mu F \ \therefore R = 1M\Omega$$

Subject : Date:

Non-linear applications:-

① The Comparator (limiter)

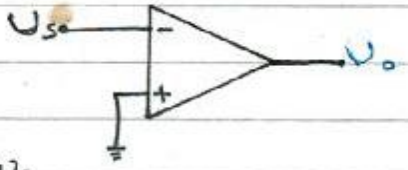


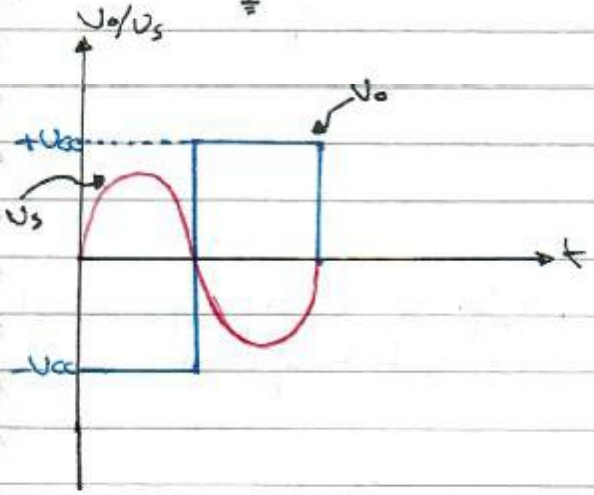
If $V_1 > V_2$

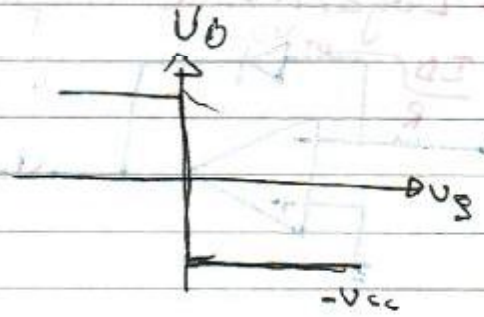
$V_o = -V_{cc}$

If $V_2 > V_1$

$V_o = +V_{cc}$







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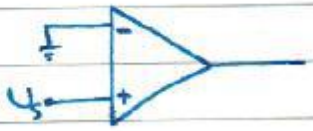

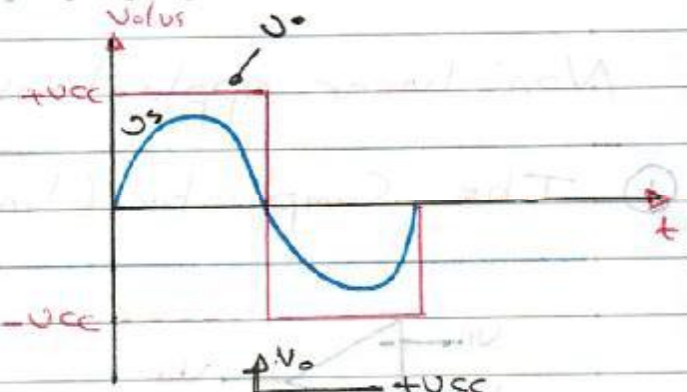

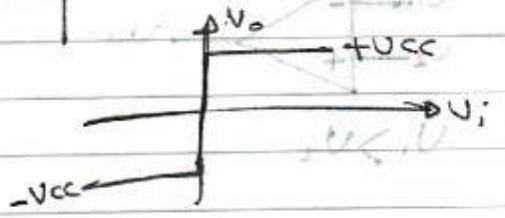

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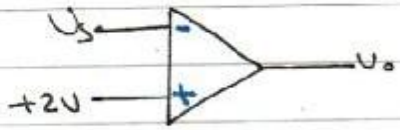
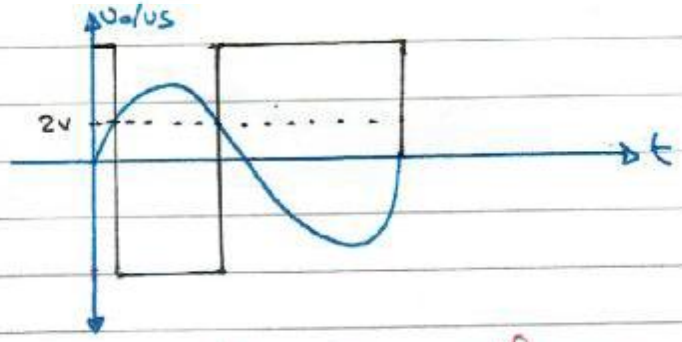
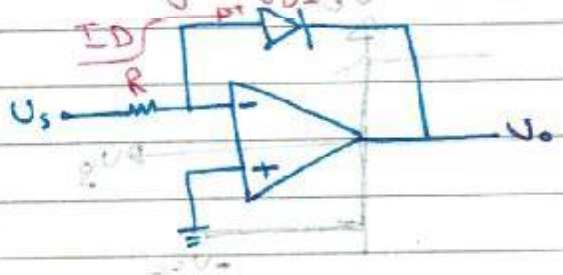


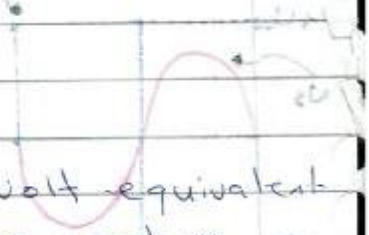


H.W

Transfer c/c's.

2- Logarithmic amplifier:-





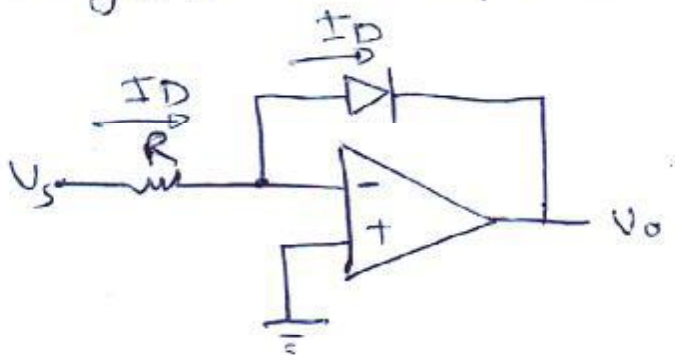
V_T = volt equivalent of temperature

$$I_D = \frac{V_S}{R}$$

$$V_D = -V_o = V_T \ln \frac{I_D}{I_S}$$

$$V_o = -V_T \ln\left(\frac{V_S}{R I_S}\right)$$

4- Logarithmic Amplifier



$$I_D = \frac{V_s}{R}$$

$$V_D = -V_o$$

$$V_o = -V_T \ln \frac{I_D}{I_s}$$

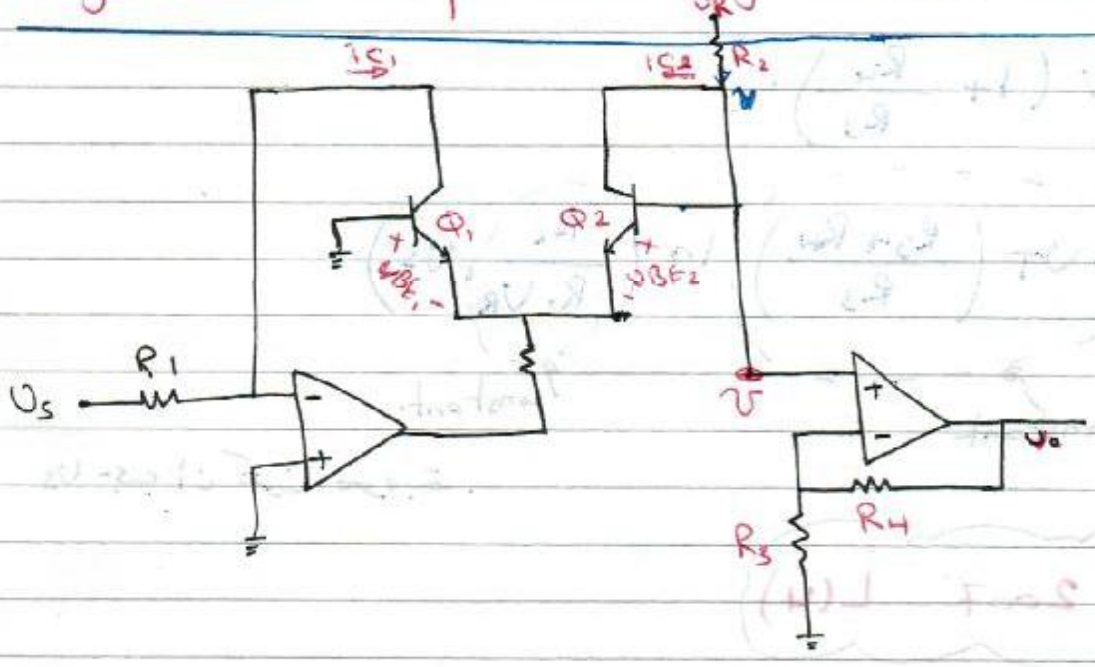
$$V_o = -V_T \ln \left(\frac{V_s}{R I_s} \right) .$$

Subject : Date:

$$V_o = -V_T \ln\left(V_S \frac{1}{RI_S}\right)$$

خلية

Logarithmic amplifier using matched transistors:-



$$V = V_{BE2} - V_{BE1}$$

$$= V_T \ln \frac{i_{C2}}{I_S} - V_T \ln \frac{i_{C1}}{I_S}$$

$$= V_T \ln \frac{i_{C2}}{i_{C1}}$$

$$= -V_T \ln \frac{i_{C1}}{i_{C2}}$$

$i_{C2} = \frac{V_R}{R_2}$, اذا أهملنا تيار الـ base

Subject: Date:

$$iC_1 = \frac{V_s}{R_1}$$

$$V = -V_T \ln\left(\frac{V_s R_2}{R_1 V_R}\right)$$

V_R is a constant.

$$V_o = V\left(1 + \frac{R_4}{R_3}\right)$$

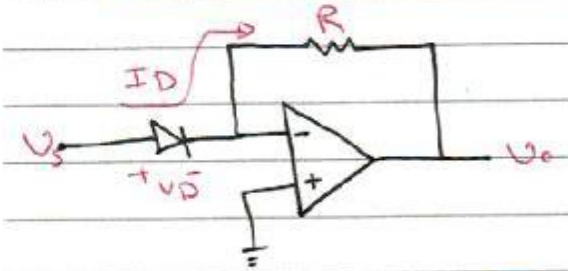
$$V_o = -V_T\left(\frac{R_3 + R_4}{R_3}\right) \ln\left(\frac{R_2}{R_1 V_R} V_s\right)$$

constant — constant

V_s يجب أن تكون موجبة.

18-11-2007 — L(4)

5. Exponential amplifier:-

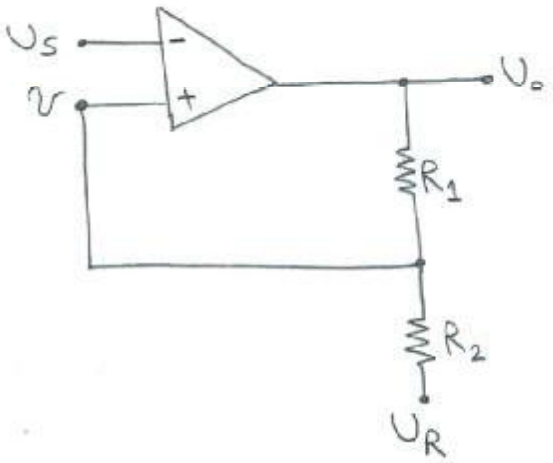


$$V_D = V_s = V_T \ln\frac{I_D}{I_s}$$

$$I_D = \frac{-V_o}{R}$$

(2) Regenerative Comparator (schmitt trigger):-

(a) Inverting schmitt trigger



Assume that $V_S < v$ so that $V_o = +E$. The voltage v can be found by using superposition:-

$$v = V_R \frac{R_1}{R_1 + R_2} + V_o \frac{R_2}{R_1 + R_2}$$

In this case $v = V_R \frac{R_1}{R_1 + R_2} + E_o \frac{R_2}{R_1 + R_2} = V_1$

$= \text{Constant.}$

If V_S increases until $V_S = V_1$, then $V_o = -E$

The transfer c/c's of this case is as in figure (a).

note: E is the saturation voltage of the op-amp.

Now $V_o = -E$ and

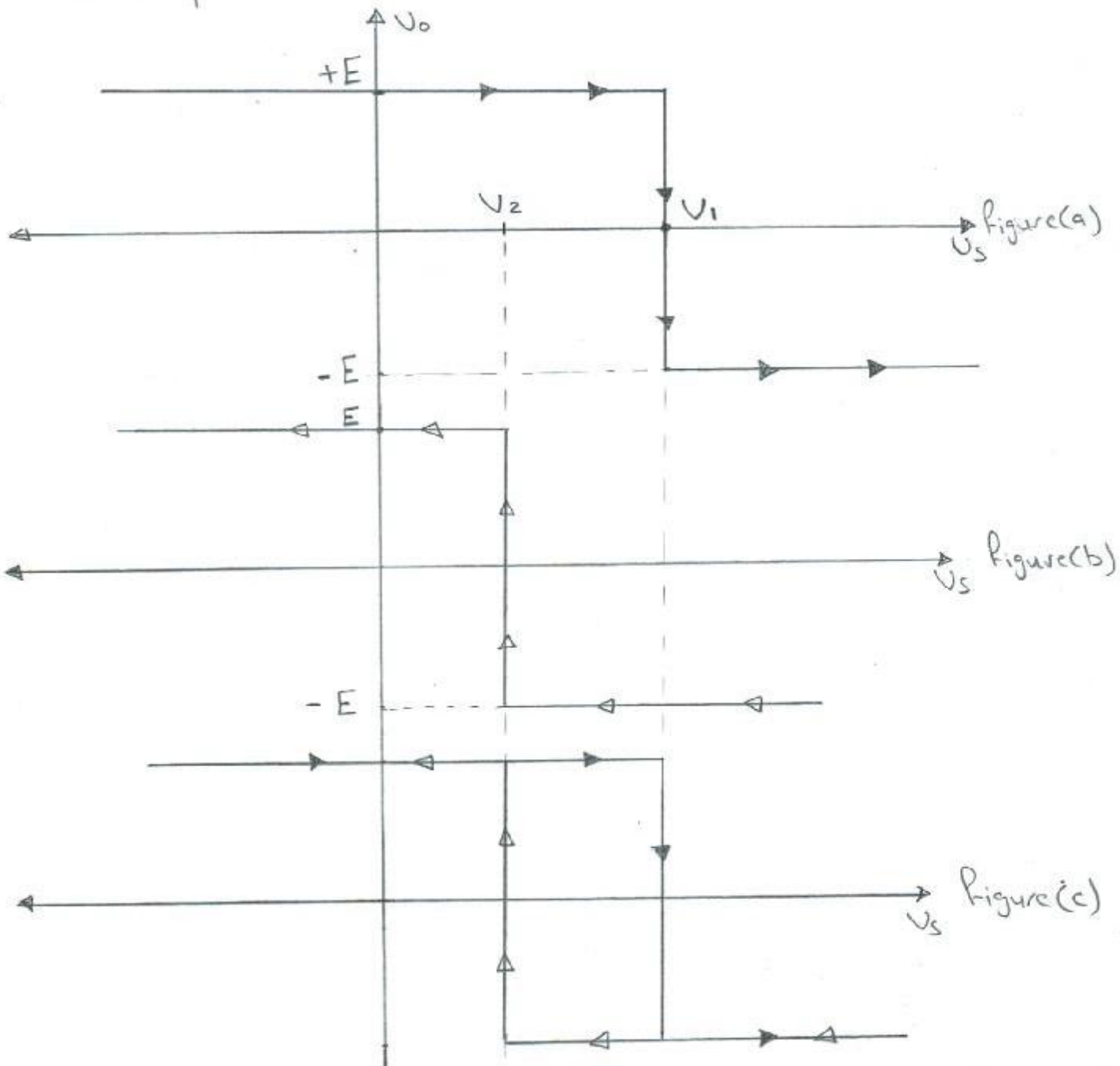
$$v = V_R \frac{R_1}{R_1 + R_2} - E \frac{R_2}{R_1 + R_2} = V_2 = \text{constant}$$

$V_2 < V_1$

If V_s decreases until $V_s = V_2$, then $V_o = +E$.

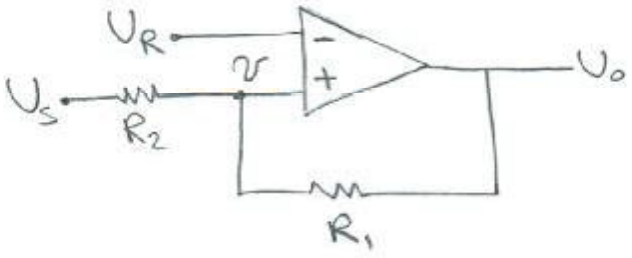
The transfer c/c's of this case is as in figure (b).

The Complete transfer c/c's is as in figure (c).



$V_H = V_1 - V_2 =$ Hysterisis

(b) Non - Inverting Schmitt trigger



Assume that $v < V_R$, $V_o = -E$,

$$v = V_s \frac{R_1}{R_1 + R_2} + V_o \frac{R_2}{R_1 + R_2}$$

In this case

$$v = V_s \frac{R_1}{R_1 + R_2} + -E \frac{R_2}{R_1 + R_2}$$

$$V_s \frac{R_1}{R_1 + R_2} - E \frac{R_2}{R_1 + R_2} < V_R$$

$$V_s < \left(V_R \frac{R_1 + R_2}{R_1} + E \frac{R_2}{R_1} \right) V_1$$

If V_s increases until $v \geq V_R$ and $V_s = V_1$ then $V_o = +E$. The transfer c/c's is as in figure (a).

Now $V_o = +E$ and

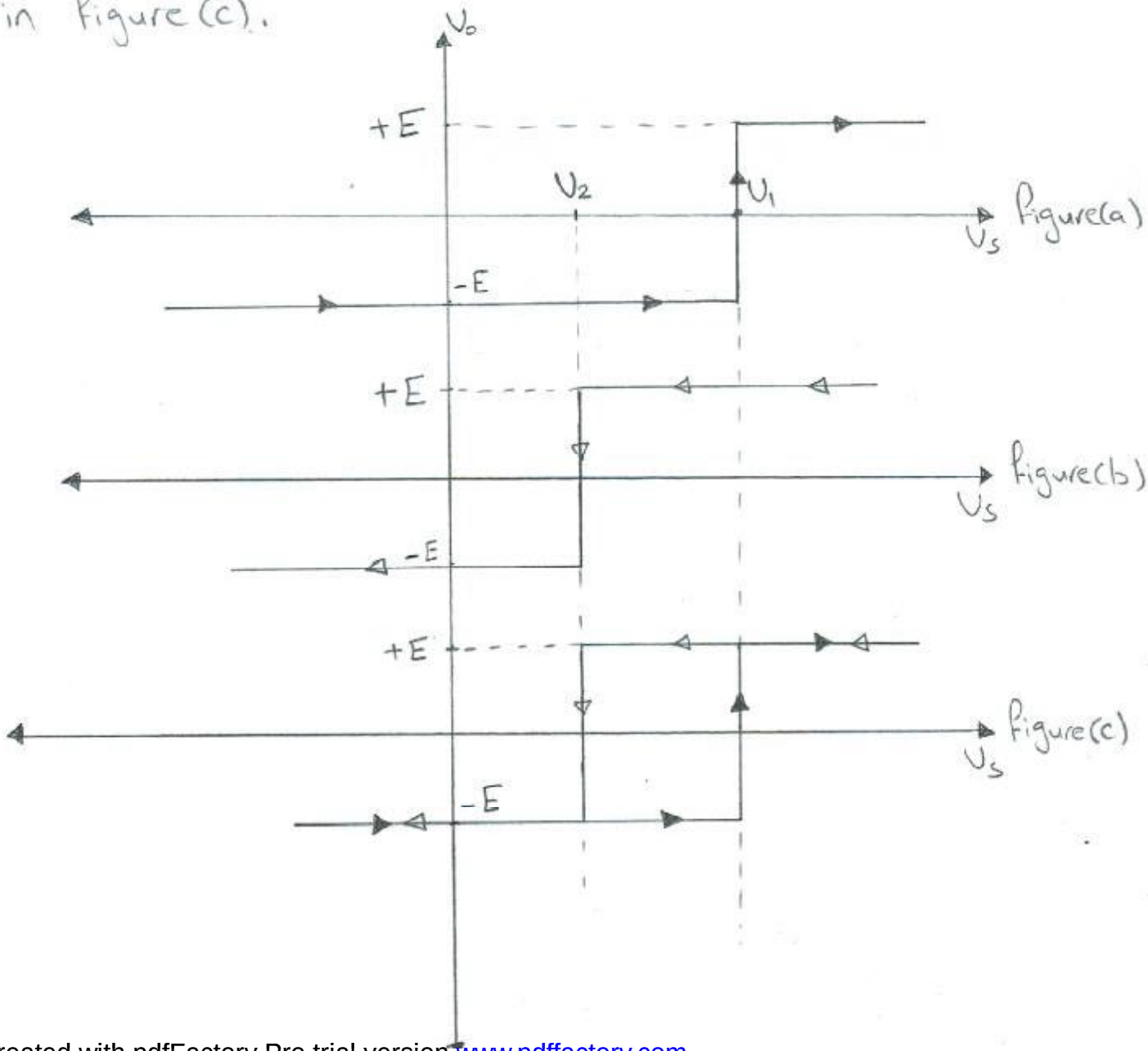
$$v = V_s \frac{R_1}{R_1 + R_2} + E \frac{R_2}{R_1 + R_2}$$

and

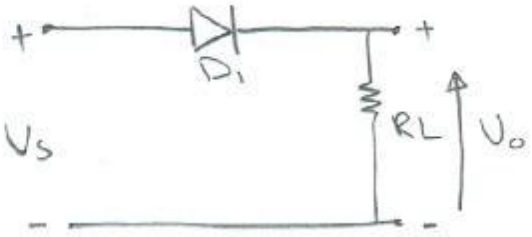
$$V_S \geq \left(V_R \frac{R_1+R_2}{R_2} - E \frac{R_1}{R_2}\right) \leftarrow V_2$$

If V_S decreases until $v \leq V_R$ and $V_S \leq V_2$ then $V_o = -E$

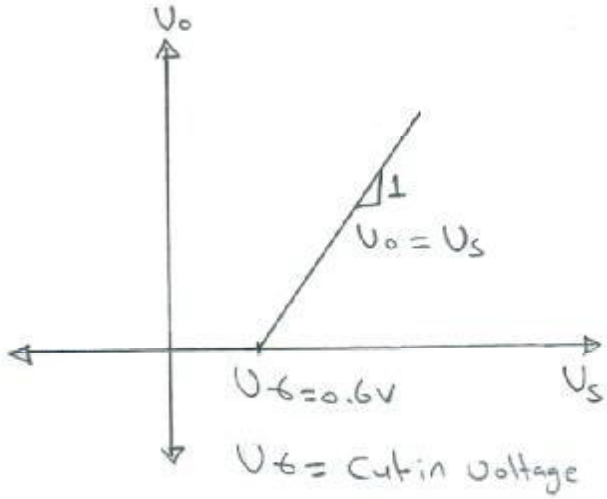
The transfer c/c's of this case is shown in figure (b). The Complete transfer c/c's is shown in figure (c).



③ Half-Wave Rectifier :-



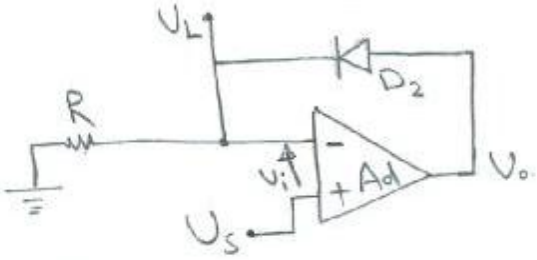
Half-Wave rectifier using a diode only.



Vγ = Cut in voltage

if $V_s < 0.6\ V$, V_o = Zero.

So we will use the following circuit to rectify voltages less than 0.6 V:-



Half-wave rectifier using an op-amp.

V_L :- the output of the rectifier

Diode D_2 is not conducting when $V_o < V_\gamma$ and $V_L = 0$.

$$A_d = \frac{V_o}{V_i} \quad , \quad V_i = V_s - V_L$$

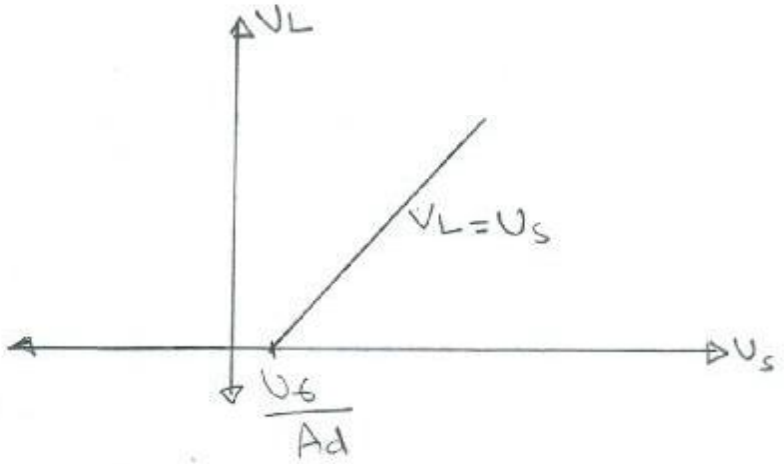
$\therefore V_i = V_s$

and $A_d V_s < V_\gamma$

$$V_s < \frac{V_\gamma}{A_d} \quad , \text{ typically } A_d = (10^5 - 10^6)$$

So if $V_s < 6\mu V$, $V_L = 0$.

Now if V_s increases until $V_o > V_\delta$ and $V_s > \frac{V_\delta}{A_d}$ then D_2 Conducts and $V_L = V_s$.



So voltages in miliVolt range can be rectified

CHAPTER 8

Feedback

INTRODUCTION

Most physical systems incorporate some form of feedback. It is interesting to note, though, that the theory of negative feedback has been developed by electronics engineers. In his search for methods for the design of amplifiers with stable gain for use in telephone repeaters, Harold Black, an electronics engineer with the Western Electric Company, invented the feedback amplifier in 1928. Since then the technique has been so widely used that it is almost impossible to think of electronic circuits without some form of feedback, either implicit or explicit. Furthermore, the concept of feedback and its associated theory is currently used in areas other than engineering, such as in the modeling of biological systems.

Feedback can be either **negative (degenerative)** or **positive (regenerative).** In amplifier design, negative feedback is applied to effect one or more of the following properties:

1. *Desensitize the gain;* that is, make the value of the gain less sensitive to variations in the value of circuit components, such as variations that might be caused by changes in temperature.

2. *Reduce nonlinear distortion:* that is, make the output proportional to the input (in other words, make the gain constant, independent of signal level).
3. *Reduce the effect of noise:* that is, minimize the contribution to the output of unwanted electric signals generated by the circuit components themselves and extraneous interference.
4. *Control the input and output impedances:* that is, raise or lower the input and output impedances by the selection of an appropriate feedback topology.
5. *Extend the bandwidth* of the amplifier.

All of the above desirable properties are obtained at the expense of a reduction in gain. It will be shown that the gain-reduction factor, called the **amount of feedback,** is the factor by which the circuit is desensitized, by which the input impedance of a voltage amplifier is increased, by which the bandwidth is extended, and so on. In short, *the basic idea of negative feedback is to trade off gain for other desirable properties.* This chapter is devoted to the study of negative-feedback amplifiers: their analysis, design, and characteristics.

Under certain conditions, the negative feedback in an amplifier can become positive and of such a magnitude as to cause oscillation. In fact, in Chapter 12 we will study the use of positive feedback in the design of oscillators and bistable circuits. In this chapter, however, we are interested in the design of stable amplifiers. We shall therefore study the stability problems of negative-feedback amplifiers and their potential for oscillation.

It should not be implied, however, that positive feedback always leads to instability. In fact, positive feedback is quite useful in a number of applications, such as the design of active filters, which are studied in Chapter 11.

Before we begin our study of negative feedback, we wish to remind the reader that we have already encountered negative feedback in a number of applications. Almost all op amp circuits employ negative feedback. Another popular application of negative feedback is the use of the emitter resistance R_E to stabilize the bias point of bipolar transistors and to increase the input resistance and bandwidth of a BJT differential amplifier. In addition, the emitter follower and the source follower employ a large amount of negative feedback. The question then arises as to the need for a formal study of negative feedback. As will be appreciated by the end of this chapter, the formal study of feedback provides an invaluable tool for the analysis and design of electronic circuits. Also, the insight gained by thinking in terms of feedback is extremely profitable.

8.1 THE GENERAL FEEDBACK STRUCTURE

Figure 8.1 shows the basic structure of a feedback amplifier. Rather than showing voltages and currents, Fig. 8.1 is a **signal-flow diagram,** where each of the quantities x can represent either a voltage or a current signal. The *open-loop* amplifier has a gain A; thus its output x_o is related to the input x_i by

$$x_o = Ax_i \tag{8.1}$$

The output x_o is fed to the load as well as to a feedback network, which produces a sample of the output. This sample x_f is related to x_o by the **feedback factor** β,

$$x_f = \beta x_o \tag{8.2}$$

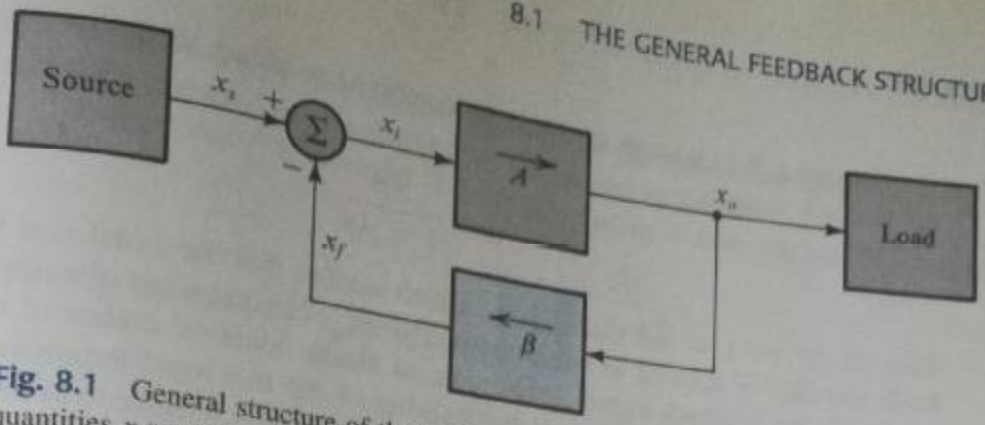


Fig. 8.1 General structure of the feedback amplifier. This is a signal-flow diagram, and the quantities x represent either voltage or current signals.

The feedback signal x_f is *subtracted* from the source signal x_s, which is the input to the complete feedback amplifier, to produce the signal x_i, which is the input to the basic amplifier,

$$x_i = x_s - x_f \tag{8.3}$$

Here we note that it is this subtraction that makes the feedback negative. In essence, negative feedback reduces the signal that appears at the input of the basic amplifier.

Implicit in the above description is that the source, the load, and the feedback network *do not* load the basic amplifier. That is, the gain A does not depend on any of these three networks. In practice this will not be the case, and we shall have to find a method for casting a real circuit into the ideal structure depicted in Fig. 8.1. Also implicit in Fig. 8.1 is that the forward transmission occurs entirely through the basic amplifier and the reverse transmission occurs entirely through the feedback network.

The gain of the feedback amplifier can be obtained by combining Eqs. (8.1) through (8.3):

$$A_f \equiv \frac{x_o}{x_s} = \frac{A}{1 + A\beta} \tag{8.4}$$

The quantity $A\beta$ is called the **loop gain,** a name that follows from Fig. 8.1. For the feedback to be negative, the loop gain $A\beta$ should be positive; that is, the feedback signal x_f should have the same sign as x_s, thus resulting in a smaller difference signal x_i. Equation (8.4) indicates that for positive $A\beta$ the gain with feedback will be smaller than the open-loop gain A by the quantity $1 + A\beta$, which is called the **amount of feedback.**

If, as is the case in many circuits, the loop gain $A\beta$ is large, $A\beta \gg 1$, then from Eq. (8.4) it follows that $A_f \simeq 1/\beta$, which is a very interesting result: *The gain of the feedback amplifier is almost entirely determined by the feedback network.* Since the feedback network usually consists of passive components, which can be chosen to be as accurate as one wishes, the advantage of negative feedback in obtaining accurate, predictable, and stable gain should be apparent. In other words the overall gain will have very little dependence on the gain of the basic amplifier, A, a desirable property because the gain A is usually a function of many parameters, some of which might have wide tolerances. We have seen a dramatic illustration of all of these results in op amp circuits, where the **closed-loop gain** (which is another name for the gain with feedback) is almost entirely determined by the feedback elements.

Equations (8.1) through (8.3) can be combined to obtain the following expression for the feedback signal x_f:

$$x_f = \frac{A\beta}{1 + A\beta} x_s$$

Thus for $A\beta \gg 1$ we see that $x_f = x_s$, which implies that the signal x_i at the input of the basic amplifier is reduced to almost zero. Thus if a large amount of negative feedback is employed, the feedback signal x_f becomes an almost identical replica of the input signal x_s. An outcome of this property is the tracking of the two input terminals of an op amp. The difference between x_s and x_f, which is x_i, is sometimes referred to as the "error signal." Accordingly, the input differencing circuit is often also called a **comparison circuit.** (It is also known as a **mixer.**)

Exercise

8.1 The noninverting op amp configuration shown in Fig. E8.1 provides a direct implementation of the feedback loop of Fig. 8.1.
(a) Assume that the op amp has infinite input resistance and zero output resistance. Find an expression for the feedback factor β. (b) If the open-loop voltage gain $A = 10^4$, find R_2/R_1 to obtain a closed-loop voltage gain A_f of 10. (c) What is the amount of feedback in decibels? (d) If $V_s = 1$ V, find V_o, V_f, and V_i. (e) If A decreases by 20%, what is the corresponding decrease in A_f?

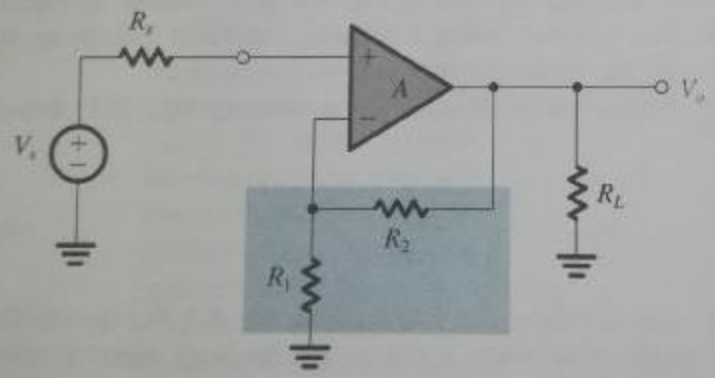


Fig. E8.1

Ans. (a) $\beta = R_1/(R_1 + R_2)$; (b) 9.01; (c) 60 dB; (d) 10 V, 0.999 V, 0.001 V; (e) 0.02%

8.2 SOME PROPERTIES OF NEGATIVE FEEDBACK

The properties of negative feedback were mentioned in the Introduction. In the following, we shall consider some of these properties in more detail.

Gain Desensitivity

The effect of negative feedback on desensitizing the closed-loop gain was demonstrated in Exercise 8.1, where we saw that a 20% reduction in the gain of the basic amplifier gave

rise to only a 0.02% reduction in the gain of the closed-loop amplifier. This sensitivity-reduction property can be analytically established as follows:

Assume that β is constant. Taking differentials of both sides of Eq. (8.4) results in

$$dA_f = \frac{dA}{(1 + A\beta)^2} \tag{8.5}$$

Dividing Eq. (8.5) by Eq. (8.4) yields

$$\frac{dA_f}{A_f} = \frac{1}{(1 + A\beta)} \frac{dA}{A} \tag{8.6}$$

which says that the percentage change in A_f (due to variations in some circuit parameter) is smaller than the percentage change in A by the amount of feedback. For this reason the amount of feedback, $1 + A\beta$, is also known as the **desensitivity factor.**

Bandwidth Extension

Consider an amplifier whose high-frequency response is characterized by a single pole. Its gain at mid and high frequencies can be expressed as

$$A(s) = \frac{A_M}{1 + s/\omega_H} \tag{8.7}$$

where A_M denotes the midband gain and ω_H is the upper 3-dB frequency. Application of negative feedback, with a frequency-independent factor β, around this amplifier results in a closed-loop gain $A_f(s)$ given by

$$A_f(s) = \frac{A(s)}{1 + \beta A(s)}$$

Substituting for $A(s)$ from Eq. (8.7) results, after a little manipulation, in

$$A_f(s) = \frac{A_M/(1 + A_M\beta)}{1 + s/\omega_H(1 + A_M\beta)}$$

Thus the feedback amplifier will have a midband gain of $A_M/(1 + A_M\beta)$ and an upper 3-dB frequency ω_{Hf} given by

$$\omega_{Hf} = \omega_H(1 + A_M\beta) \tag{8.8}$$

It follows that the upper 3-dB frequency is increased by a factor equal to the amount of feedback.

Similarly, it can be shown that if the open-loop gain is characterized by a dominant low-frequency pole giving rise to a lower 3-dB frequency ω_L, then the feedback amplifier will have a lower 3-dB frequency ω_{Lf},

$$\omega_{Lf} = \frac{\omega_L}{1 + A_M\beta} \tag{8.9}$$

Note that the amplifier bandwidth is increased by the same factor by which its midband gain is decreased, maintaining the gain–bandwidth product constant.

Exercise

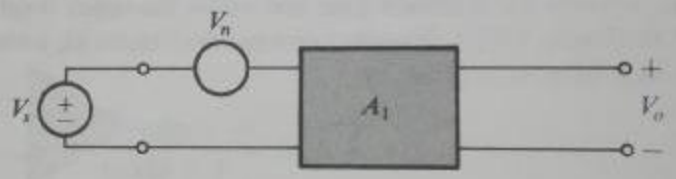
8.2 Consider the noninverting op-amp circuit of Exercise 8.1. Let the open-loop gain A have a low-frequency value of 10^4 and a uniform -6 dB/octave rolloff at high frequencies with a 3-dB frequency of 100 Hz. Find the low-frequency gain and the upper 3-dB frequency of a closed-loop amplifier with $R_1 = 1\ \text{k}\Omega$ and $R_2 = 9\ \text{k}\Omega$.

Ans. 9.99 V/V; 100.1 kHz

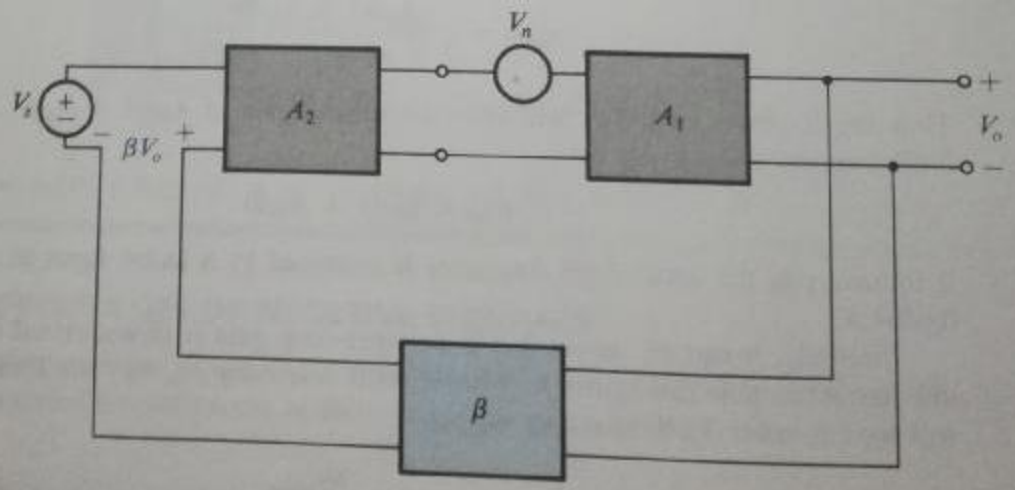
Noise Reduction

Negative feedback can be employed to reduce the noise or interference in an amplifier or, more precisely, to increase the ratio of signal to noise. However, as we shall now explain, this noise-reduction process is possible only under certain conditions. Consider the situation illustrated in Fig. 8.2. Figure 8.2(a) shows an amplifier with gain A_1, an input signal V_s, and noise, or interference, V_n. It is assumed that for some reason this amplifier suffers from noise and that the noise can be assumed to be introduced at the input of the amplifier. The **signal-to-noise ratio** for this amplifier is

$$S/N = V_s/V_n$$



(a)



(b)

Fig. 8.2 Illustrating the application of negative feedback to improve the signal-to-noise ratio in amplifiers.

Consider next the circuit in Fig. 8.2(b). Here we assume that it is possible to build another amplifier stage with gain A_2 that does not suffer from the noise problem. If this is the case, then we may precede our original amplifier A_1 by the *clean* amplifier A_2 and apply negative feedback around the overall cascade of such an amount as to keep the overall gain constant. The output voltage of the circuit in Fig. 8.2(b) can be found by superposition:

$$V_o = V_s \frac{A_1 A_2}{1 + A_1 A_2 \beta} + V_n \frac{A_1}{1 + A_1 A_2 \beta}$$

Thus the signal-to-noise ratio at the output becomes

$$\frac{S}{N} = \frac{V_s}{V_n} A_2$$

which is A_2 times higher than in the original case.

We should emphasize once more that the improvement in signal-to-noise ratio by the application of feedback is possible only if one can precede the noisy stage by a (relatively) noise-free stage. This situation, however, is not uncommon in practice. The best example is found in the output power-amplifier stage of an audio amplifier. Such a stage usually suffers from a problem known as **power-supply hum.** The problem arises because of the large currents that this stage draws from the power supply and the difficulty in providing adequate power-supply filtering inexpensively.

The power-output stage is required to provide large power gain but little or no voltage gain. We may therefore precede the power-output stage by a small-signal amplifier that provides large voltage gain, and apply a large amount of negative feedback, thus restoring the voltage gain to its original value. Since the small-signal amplifier can be fed from another, less hefty (and hence better regulated) power supply, it will not suffer from the hum problem. The hum at the output will then be reduced by the amount of the voltage gain of this added **preamplifier.**

Exercise

8.3 Consider a power-output stage with voltage gain $A_1 = 1$, an input signal $V_s = 1$ V, and a hum V_n of 1 V. Assume that this power stage is preceded by a small-signal stage with gain $A_2 = 100$ V/V and that overall feedback with $\beta = 1$ is applied. If V_s and V_n remain unchanged, find the signal and noise voltages at the output and hence the improvement in S/N.

Ans. ≃1 V; ≃0.01 V; 100 (40 dB)

Reduction in Nonlinear Distortion

Curve (a) in Fig. 8.3 shows the transfer characteristic of an amplifier. As indicated, the characteristic is piecewise linear, with the voltage gain changing from 1000 to 100 and then to 0. This nonlinear transfer characteristic will result in this amplifier generating a large amount of nonlinear distortion.

The amplifier transfer characteristic can be considerably **linearized** (that is, made less nonlinear) through the application of negative feedback. That this is possible should not be

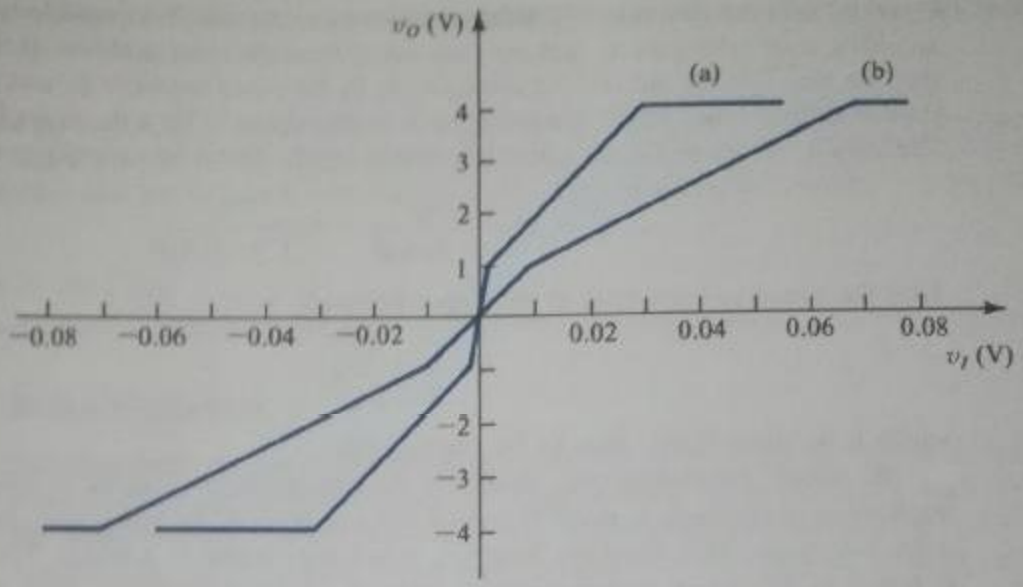


Fig. 8.3 Illustrating the application of negative feedback to reduce the nonlinear distortion in amplifiers. Curve (a) shows the amplifier transfer characteristic without feedback. Curve (b) shows the characteristic with negative feedback ($\beta = 0.01$) applied.

too surprising, since we have already seen that negative feedback reduces the dependence of the overall closed-loop amplifier gain on the open-loop gain of the basic amplifier. Thus large changes in open-loop gain (1000 to 100 in this case) give rise to much smaller corresponding changes in the closed-loop gain.

To illustrate, let us apply negative feedback with $\beta = 0.01$ to the amplifier whose open-loop voltage transfer characteristic is depicted in Fig. 8.3. The resulting transfer characteristic of the closed-loop amplifier is shown in Fig. 8.3 as curve (b). Here the slope of the steepest segment is given by

$$A_{f1} = \frac{1000}{1 + 1000 \times 0.01} = 90.9$$

and the slope of the next segment is given by

$$A_{f2} = \frac{100}{1 + 100 \times 0.01} = 50$$

Thus the order-of-magnitude change in slope has been considerably reduced. The price paid, of course, is a reduction in voltage gain. Thus if the overall gain has to be restored, then a preamplifier should be added. This preamplifier should not present a severe nonlinear distortion problem, since it will be dealing with smaller signals.

Finally, it should be noted that negative feedback does nothing about amplifier saturation, since in saturation the gain is very small (almost zero) and hence the amount of feedback is also very small (almost zero).

8.3 THE FOUR BASIC FEEDBACK TOPOLOGIES

Based on the quantity to be amplified (voltage or current) and on the desired form of output (voltage or current), amplifiers can be classified into four categories. These categories were discussed in Chapter 1. In the following, we shall review this amplifier classification and point out the feedback topology appropriate in each case.

Voltage Amplifiers

Voltage amplifiers are intended to amplify an input voltage signal and provide an output voltage signal. The voltage amplifier is essentially a voltage-controlled voltage source. The input impedance is required to be high, and the output impedance is required to be low. Since the signal source is essentially a voltage source, it is convenient to represent it in terms of a Thévenin equivalent circuit. In a voltage amplifier the output quantity of interest is the output voltage. It follows that the feedback network should *sample* the output *voltage*. Also, because of the Thévenin representation of the source, the feedback signal x_f should be a voltage that can be *mixed* with the source voltage in *series*.

A suitable feedback topology for the voltage amplifier is the **voltage-sampling series-mixing** one shown in Fig. 8.4(a). As will be shown, this topology not only stabilizes the voltage gain but also results in a higher input resistance (intuitively, a result of the series connection at the input) and a lower output resistance (intuitively, a result of the parallel connection at the output), which are desirable properties for a voltage amplifier. The non-inverting op-amp configuration of Fig. E8.1 is an example of this feedback topology. Finally, it should be mentioned that this feedback topology is also known as **series–shunt feedback,** where "series" refers to the connection at the input and "shunt" refers to the connection at the output.

Current Amplifiers

Here the input signal is essentially a current, and thus the signal source is most conveniently represented by its Norton equivalent. The output quantity of interest is current; hence the feedback network should *sample* the output *current*. The feedback signal should be in current form so that it may be *mixed* in *shunt* with the source current. Thus the feedback topology suitable for a current amplifier is the **current-sampling shunt-mixing** topology, illustrated in Fig. 8.4(b). As will be shown, this topology not only stabilizes the current gain but also results in a lower input resistance and a higher output resistance, desirable properties for a current amplifier.

An example of the current-sampling shunt-mixing feedback topology is given in Fig. 8.5. Note that the bias details are not shown. Also note that the current being sampled is not the output current but the almost equal emitter current of Q_2. This is done for circuit design convenience and is quite usual in circuits involving current sampling.

The reference direction indicated in Fig. 8.5 for the feedback current I_f is such that it subtracts from I_s. This reference notation will be followed in all circuits in this chapter, since it is consistent with the notation used in the general feedback structure of Fig. 8.1. Therefore, in all circuits, for the feedback to be negative the loop gain $A\beta$ should be positive. The reader is urged to verify that in the circuit of Fig. 8.5, A is negative and β is negative.

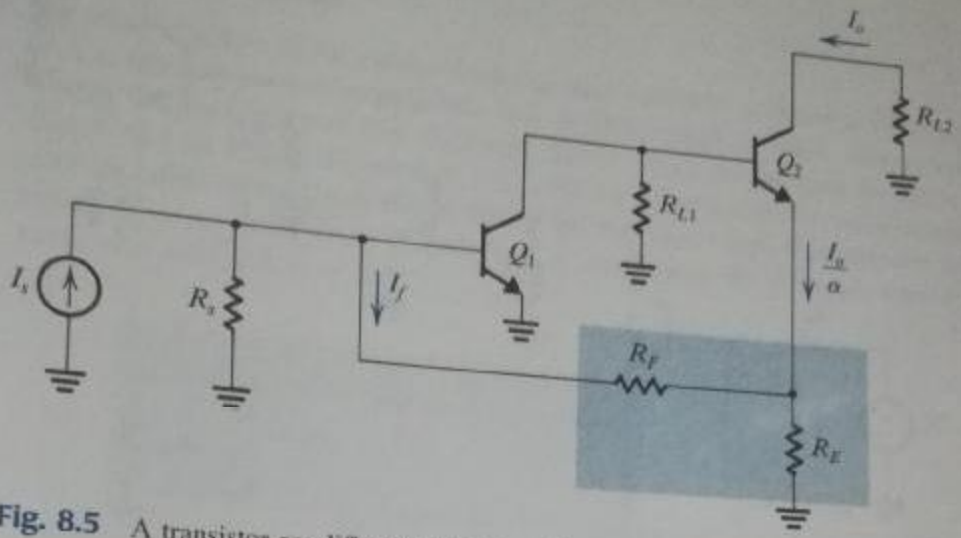


Fig. 8.5 A transistor amplifier with shunt–series feedback.

It is of utmost importance to be able to ascertain qualitatively the feedback polarity (positive or negative). This can be done by "following the signal around the loop." For instance, let the current I_s in Fig. 8.5 increase. We see that the base current of Q_1 will increase, and thus its collector current will also increase. This will cause the collector voltage of Q_1 to decrease, and thus the collector current of Q_2, I_o, will decrease. Thus the emitter current of Q_2, I_o/α (where α is the common-base current gain of the BJT), decreases. From the feedback network we see that if I_o/α decreases, then I_f (in the direction shown) will increase. The increase in I_f will subtract from I_s, causing a smaller increment to be seen by the amplifier. Hence the feedback is negative.

Finally, we should mention that this feedback topology is also known as **shunt–series feedback.** Again, the first word in the name (shunt) refers to the connection at the input, and the second word (series) refers to the connection at the output.

Transconductance Amplifiers

Here the input signal is a voltage and the output signal is a current. It follows that the appropriate feedback topology is the **current-sampling series-mixing** topology, illustrated in Fig. 8.4(c).

An example of this feedback topology is given in Fig. 8.6. Here, note that as in the circuit of Fig. 8.5 the current sampled is not the output current but the almost equal emitter current of Q_3. In addition, the mixing loop is not a conventional one; it is not a simple series connection, since the feedback signal developed across R_{E1} is in the emitter circuit of Q_1, while the source is in the base circuit of Q_1. These two approximations are done for convenience of circuit design.

Finally, it should be mentioned that the current-sampling series-mixing feedback topology is also known as the **series–series** feedback configuration.

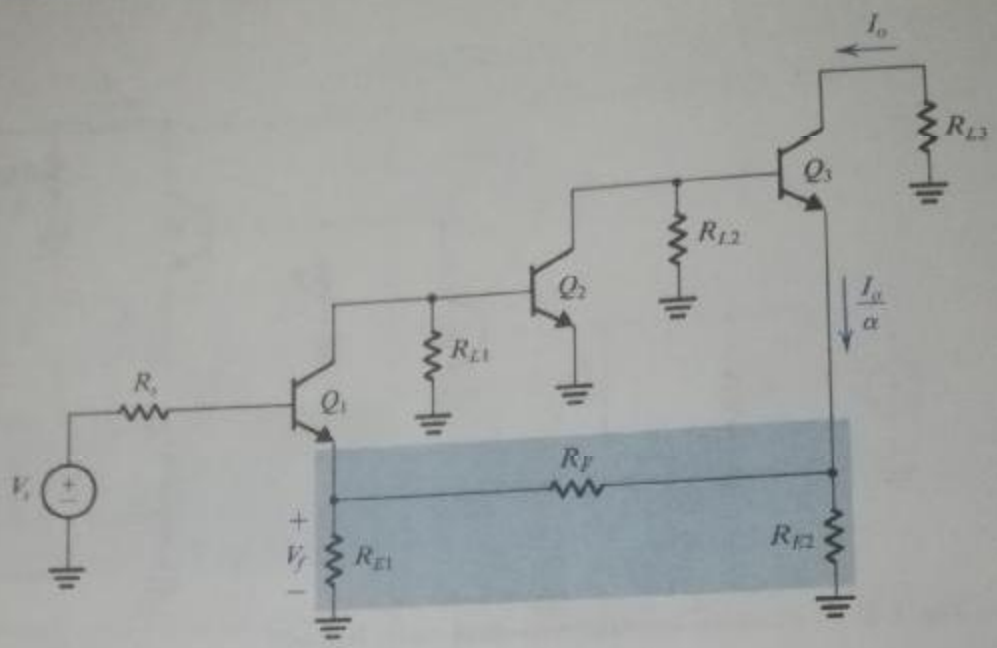


Fig. 8.6 An example of the series–series feedback topology.

Transresistance Amplifiers

Here the input signal is current and the output signal is voltage. It follows that the appropriate feedback topology is of the **voltage-sampling shunt-mixing** type, shown in Fig. 8.4(d).

An example of this feedback topology is found in the inverting op amp configuration of Fig. 8.7(a). The circuit is redrawn in Fig. 8.7(b) with the source converted to Norton's form.

This feedback topology is also known as **shunt–shunt** feedback.

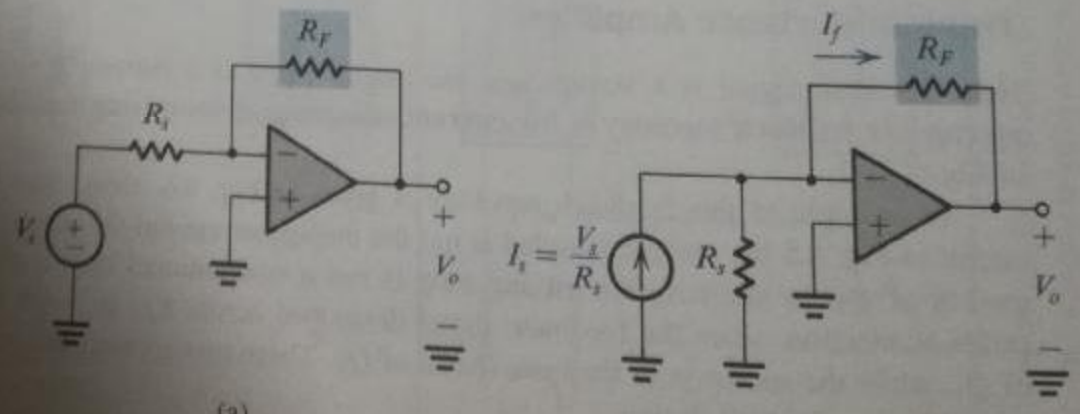


Fig. 8.7 The inverting op-amp configuration as an example of shunt–shunt feedback.

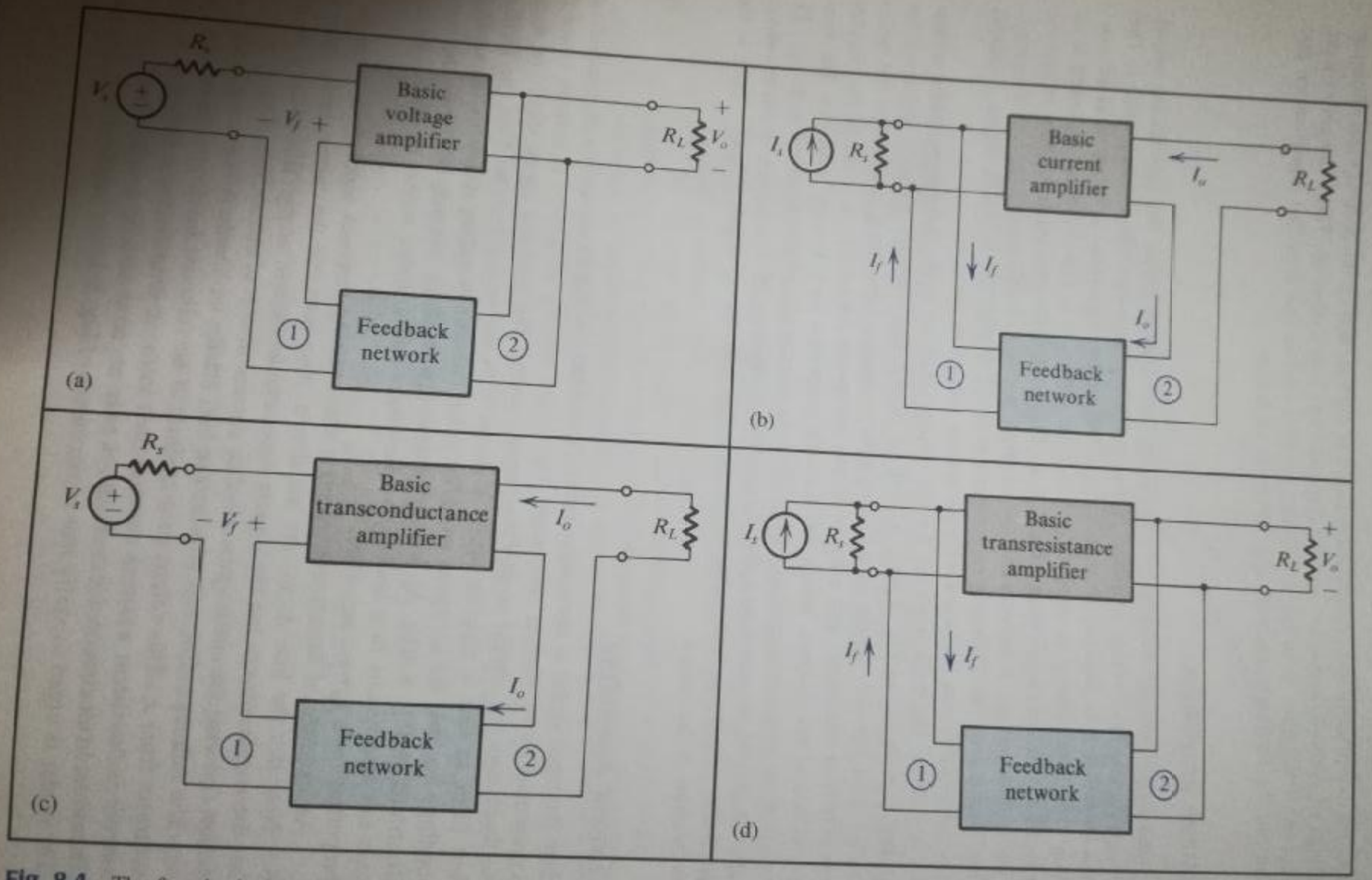


Fig. 8.4 The four basic feedback topologies: **(a)** voltage-sampling series-mixing (series–shunt) topology; **(b)** current-sampling shunt-mixing (shunt–series) topology; **(c)** current-sampling series-mixing (series–series) topology; **(d)** voltage-sampling shunt-mixing (shunt–shunt) topology.

Subject : Date:

* $R_{of}' = \frac{R_o'}{D}$

$R_o' = 4.7k \,//\, (4.7k + 0.1k)$

$= 2.37k\Omega$.

$R_{of}' = \frac{2.37k}{18.4} = 129\Omega$.

Oscillators :-

Linear Oscillators :-

An oscillator generates a periodic output without requiring any input.

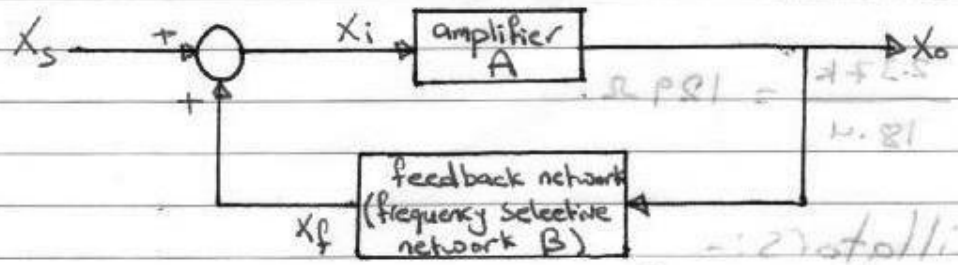
Oscillators

- Linear (sinusoidal)
- non linear (square, triangular)

Subject : Date:

Basic principles of sinusoidal oscillators:-

① The oscillator feedback loop.



The basic structure of a sinusoidal oscillator.

The frequency selective network determines the frequency of oscillation.

This is a +ve feedback structure its equations are:-

$$X_o = A X_i \quad \text{---(1)}$$

$$X_f = \beta X_o \quad \text{---(2)}$$

$$X_i = X_s + X_f \quad \text{---(3)}$$

Solving the above equations for $A_f = \frac{X_o}{X_s}$ we get:-

$$A_f = \frac{A}{1 \ominus \beta A}$$

↓ The $\ominus$ sign is for +ve feedback.

Subject : Date:

$$A_f(s) = \frac{A(s)}{1 - \beta(s)A(s)}$$

in general A does not depend on frequency.

$\beta(s)$ depends on frequency since it contains reactive elements.

the loop gain is βA.

② The Oscillation Criterian :-

If at a specific frequency the loop gain $\beta A = 1$ then :-

$$1 - \beta A = 0$$

and $A_f = \infty$

This means that we have a finite output for zero input which is by definition an oscillator.

Therefore the circuit oscillates at a frequency ω_o if :-

$$\boxed{A(j\omega_o)\beta(j\omega_o) = 1}$$

Subject : Date:

The Barkhausen criterian for oscillation is :-

1- $|A(j\omega_o)\,\beta(j\omega_o)| = 1$

2- $\angle A(j\omega_o)\,\beta(j\omega_o) = 0°$

By this we have :-

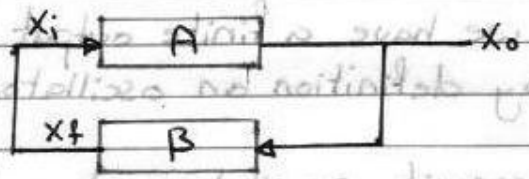
$A\beta = 1$

$X_o = A X_i$

$X_f = \beta X_o$

$\therefore X_f = A\beta X_i$, $A\beta = 1$

$\therefore \boxed{X_f = X_i}$ (no input).

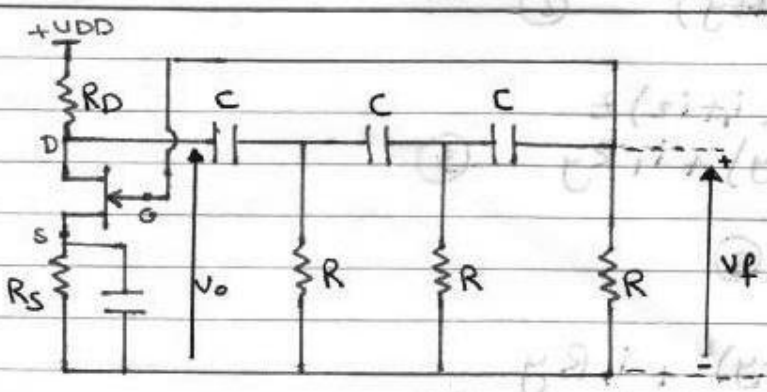


let

$|A\beta|$ 5% greater than unity to start and maintain Oscillation.

Subject : Date:

The FET phase-shift oscillator:-



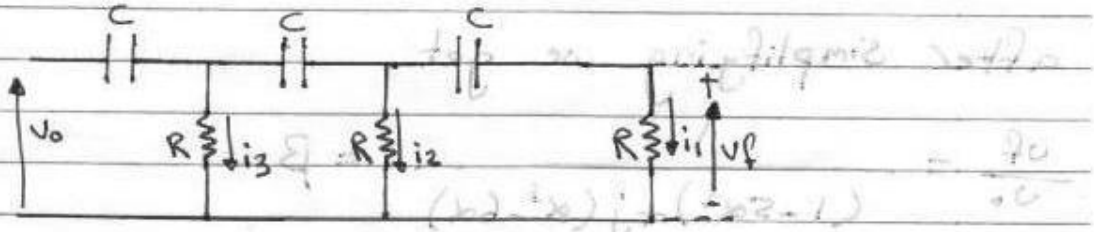
To find the frequency of oscillation:-

$A(j\omega)\beta(j\omega) = ?$

① Find $\beta(j\omega) = ?$ $\beta = \frac{v_f}{v_o}$

② Set the imaginary part = 0 and derive f_{osc}.

so for this circuit we have:-



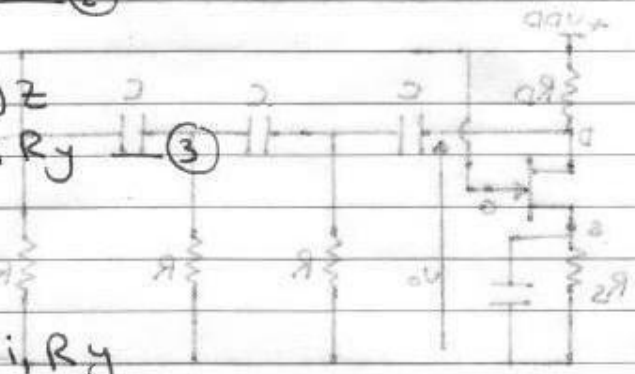
let $z = \frac{1}{j\omega C}$ and $y = \frac{z}{R}$ and $\alpha = \frac{1}{\omega CR}$

$V_f = i_1 R$ —— ①

Subject : Date:

$i_2 R = i_1(R+z)$

$i_2 R = i_1 R(1+y)$ —— (2)



$i_3 R = i_2 R + (i_1+i_2) z$

$i_3 R = i_2 R(1+y) + i_1 Ry$ —— (3)

sub (2) in (3)

$i_3 R = i_1 R(1+y)^2 + i_1 Ry$

$i_3 R = i_1 R((1+y)^2 + y)$ —— (4)

$v_o = i_3 R + (i_1 + i_2 + i_3) z$

$v_o = i_3 R(1+y) + i_1 Ry + i_2 Ry$ —— (5)

sub (4) and (2) in (5) we get

$v_o = i_1 R((1+y)^2+y)(1+y) + i_1 Ry + i_1 R(1+y)y$

after simplifying we get

$$\frac{v_f}{v_o} = \frac{}{(1-5\alpha^2)+j(\alpha^3-6\alpha)}$$

to find ω_{osc} set the imaginary part $=0$

$\alpha^3 - 6\alpha = 0 \Rightarrow \alpha = \sqrt{6}$, $\alpha = \frac{1}{\omega CR}$

$$\frac{1}{\omega_{osc} CR} = \sqrt{6} \Rightarrow \omega_{osc} = \frac{1}{\sqrt{6}\,CR}$$

Subject : Date:

$$f_{osc} = \frac{1}{2\pi\sqrt{6}\,CR}$$

$|AB| > 1$

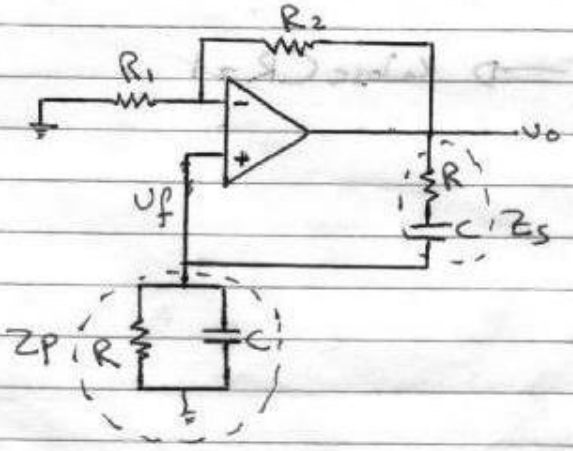
at f_{osc}

$$\beta = \frac{1}{1 - 5\alpha^2} = \frac{-1}{29}$$ -Ve and real

$$|A| \geq \frac{1}{|\beta|} \quad \therefore |A| > 29$$

$$A = \frac{-\mu R_D}{r_d + R_D} \quad \therefore \frac{-\mu R_D}{r_d + R_D} > -29$$

The Wien bridge Oscillator:-



Subject : Date:

$$A(s)\,\beta(s) = \left(1+\frac{R_2}{R_1}\right)\left(\frac{Z_p}{Z_p+Z_s}\right)$$

$$= \left(1+\frac{R_2}{R_1}\right)\left[\frac{\frac{R}{1+SCR}}{\frac{R}{1+SCR}+R+\frac{1}{SC}}\right]$$

$$= \left(1+\frac{R_2}{R_1}\right)\left(\frac{1}{3+SCR+\frac{1}{SCR}}\right)$$

$$A(j\omega)\,\beta(j\omega) = \left(1+\frac{R_2}{R_1}\right)\left[\frac{1}{3+j\left(\omega CR-\frac{1}{\omega CR}\right)}\right]$$

At ω_{osc}, imaginary part = 0

$$\omega_{osc}CR - \frac{1}{\omega_{osc}CR} = 0$$

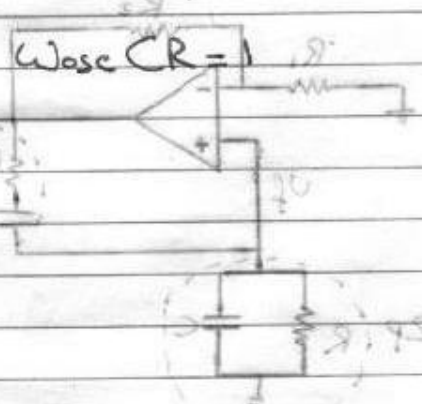
$$\left[\omega_{osc}CR\right] = \frac{1}{\omega_{osc}CR} \Rightarrow \omega_{osc}CR = 1$$

$$\omega_{osc} = \frac{1}{CR}$$

$$f_{osc} = \frac{1}{2\pi CR}$$

At ω_{osc}

$$A\beta = \left(1+\frac{R_2}{R_1}\right)\left(\frac{1}{3}\right)$$



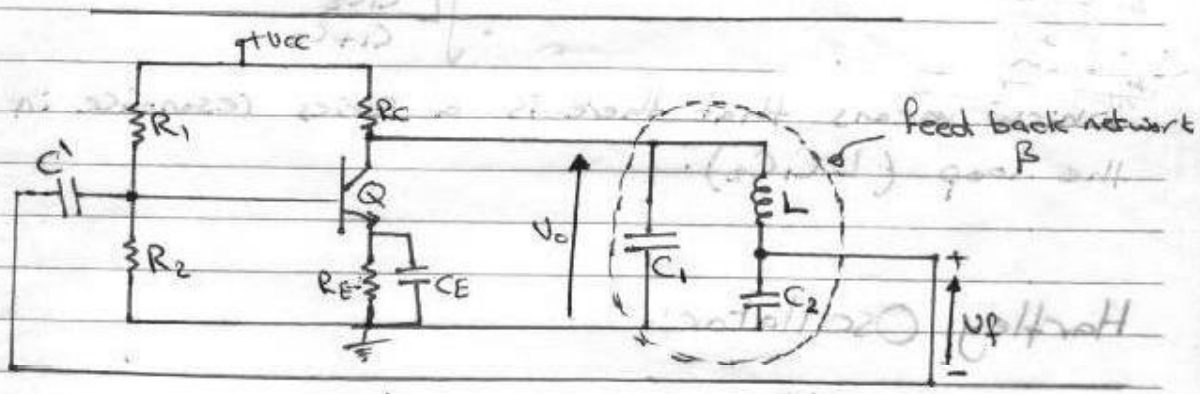
Subject :

$|AB| > 1$

$\left(1 + \frac{R_2}{R_1}\right)\left(\frac{1}{3}\right) > 1 \Longrightarrow \frac{R_2}{R_1} > 2.$

LC oscillators:-

1- The transistor colpitts oscillator:-



$$\frac{V_f}{V_o} = \beta = \frac{\frac{1}{SC_2}}{\frac{1}{SC_2} + SL} = \frac{1}{1 + S^2 LC_2}$$

$C_1, C_2 \ll C_{CE}$

$$A = \frac{V_o}{V_\pi} = \frac{-g_m V_\pi \left(R \,||\, \frac{1}{SC_1} \,||\, \left(\frac{1}{SC_2} + SL\right)\right)}{V_\pi}$$

i.e, V_{BE}.

After simplification:-

$$A\beta = -g_m \frac{R(S^2LC_2 + 1)}{SRC_2 + (SRC_1 + 1)(S^2LC_2 + 1)} * \frac{1}{(1 + S^2LC_2)}$$

Subject : Date:

$$A(j\omega)\beta(j\omega) = -g_m R\left(\frac{1}{j\omega RC_2 - j\omega^3 RLC_1C_2 + j\omega RC_1 - \omega^2 LC_2 + 1}\right)$$

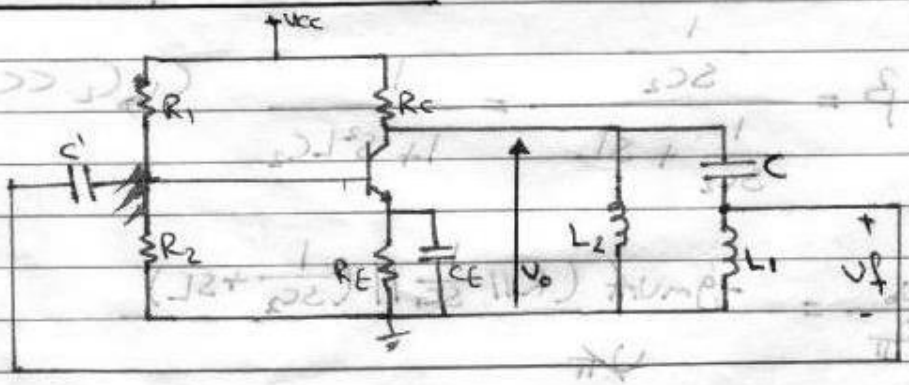
at ω_{osc}, imaginary part = 0

$$\omega_{osc} RC_2 + \omega_{osc} RC_1 - \omega_{osc}^3 RLC_1C_2 = 0$$

$$C_2 + C_1 = \omega_{osc}^2 C_1C_2L \Rightarrow \omega_{osc} = \frac{1}{\sqrt{L\frac{C_1C_2}{C_1+C_2}}}$$

which means that there is a series resonance in the loop (LC_1C_2).

Hartley Oscillator:-



$$\beta = \frac{v_f}{v_o} = \frac{sL_1}{sL_1 + \frac{1}{sC}} = \frac{s^2L_1C}{s^2L_1C + 1}$$

$$A = \frac{v_o}{v_\pi} = \frac{-g_m v_\pi (R \| sL_2 \| (sL_1 + \frac{1}{sC}))}{v_\pi}$$

Subject : Date:

after simplification, we get

$$A\beta = -g_m \left(\frac{S^3 R L_1 L_2 C}{S^2(RCL_2 + L_1 CR) + R + S^3 L_1 L_2 C + SL_2} \right)$$

$$A\beta = -g_m \left(\frac{S^2 R L_1 L_2 C}{S(RCL_2 + L_1 CR) + \frac{R}{S} + S^2 L_1 L_2 C + L_2} \right)$$

at ω_{osc}, imaginary part = 0 we get:-

$$\omega_{osc} RCL_2 + \omega_{osc} L_1 CR = \frac{R}{\omega_{osc}}$$

$$CL_2 + CL_1 = \frac{1}{\omega_{osc}^2}$$

$$\omega_{osc}^2 = \frac{1}{C(L_2 + L_1)} \Longrightarrow \omega_{osc} = \frac{1}{\sqrt{C(L_2 + L_1)}}$$

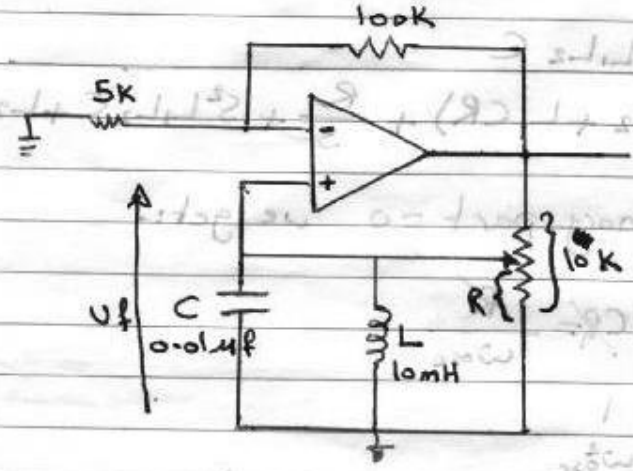
also series resonance between them.

Subject : Date:

15-19 ne2 Millman

Example: (1) 17.32 (Millman):

For the oscillator shown find the frequency of oscillation, and the minimum value of R.



$$A\beta = \left(1 + \frac{100k}{5K}\right) * \frac{Z}{Z + (10^{4} - R)}$$

$$Z = \frac{1}{j\omega C + \frac{1}{j\omega L} + \frac{1}{R}}$$

Substitute Z in the Aβ equation and set the imaginary part to zero to find fosc.

we get :-

$$f_{osc} = \frac{1}{2\pi\sqrt{LC}}$$ which is the resonance frequency for LC.

Subject : Date:

$$Z_{ip} = \frac{j\omega L * \frac{1}{j\omega C}}{j(\omega L - \frac{1}{\omega C})} = \infty$$

$$Z_{is} = j(\omega L - \frac{1}{\omega C}) = 0$$

at resonance.

at resonance

$$\therefore f_{osc} = \frac{1}{2\pi\sqrt{LC}}$$

$$= \frac{1}{2\pi\sqrt{10 * 10^{-3} * 0.01 * 10^{-6}}} = 15.92\,kHz.$$

At f_{osc}, $Z = R$.

$$\beta = \frac{R}{10^4}, \quad A = 1 + \frac{100}{5} = 21$$

$$(21)\left(\frac{R}{10^4}\right) > 1$$

$$R > \frac{10^4}{21} \Rightarrow R > 476\ \Omega$$

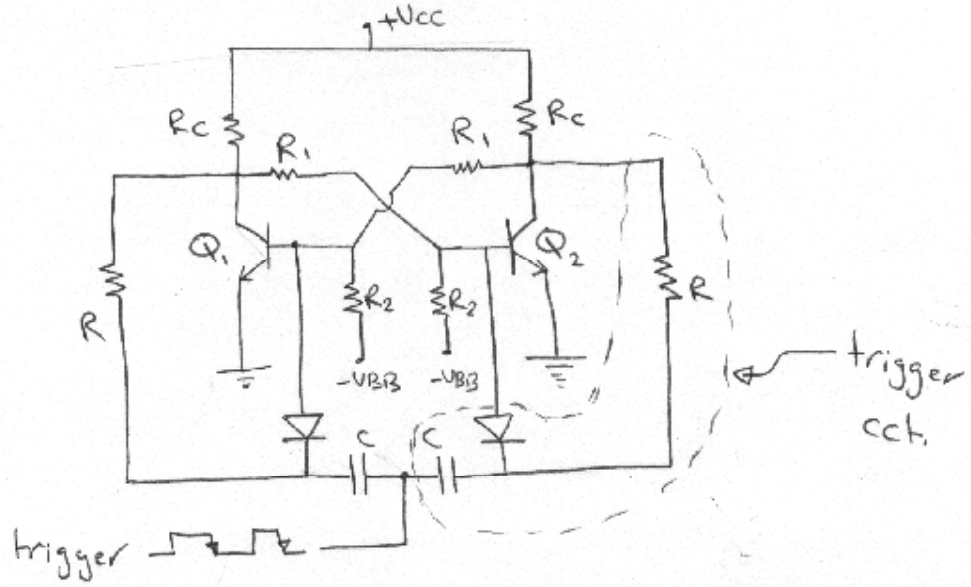
$$\therefore R_{min} = 476.$$

(d)

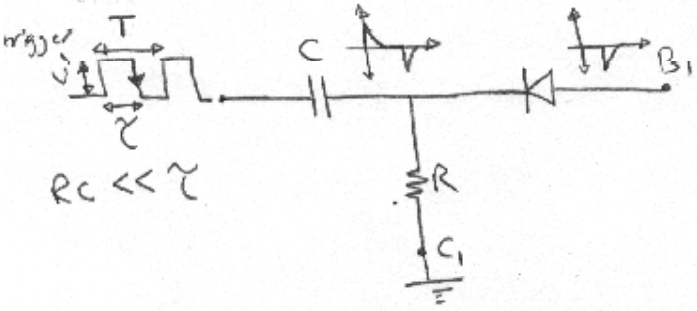
ABC

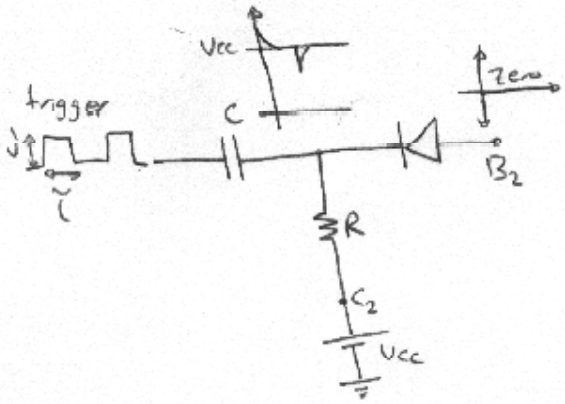
Multivibrators

1) Bistable Multivibrators :-



Assume Q_1 ON and Q_2 off.

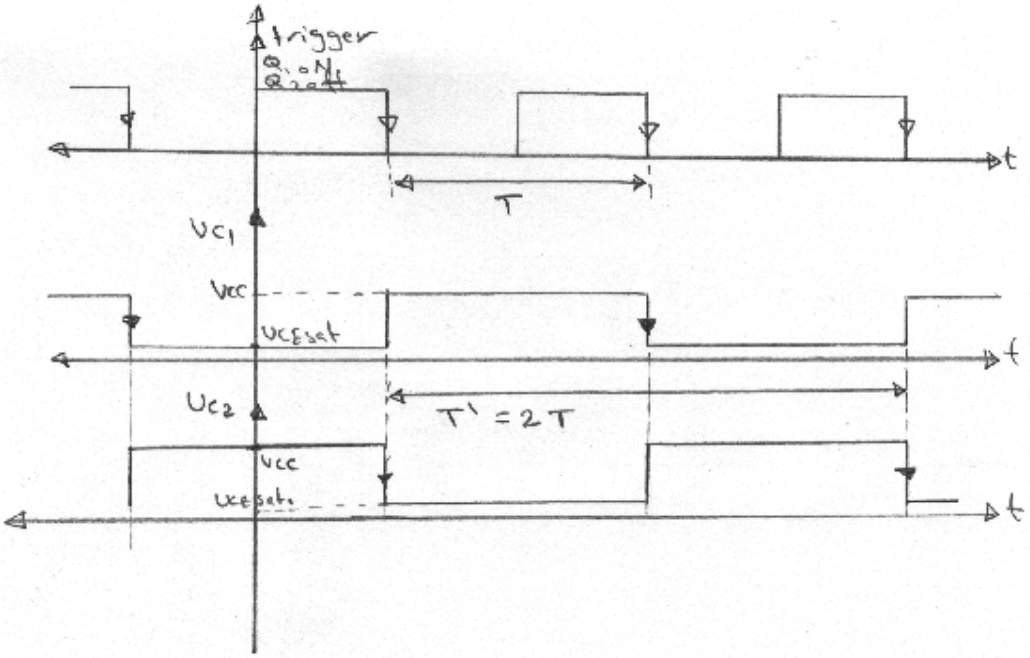


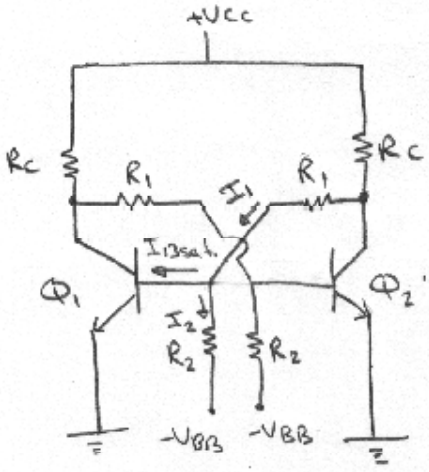


The Bistable multivibrator has two stable states :-

① when Q_1 ON , Q_2 off.

② when Q_1 off , Q_2 ON.





In order to design this circuit, assume on of the transistors are ON and the other off, so let Q_1 ON and Q_2 off.

$$R_c = \frac{V_{cc} - V_{CEsat.}}{I_{csat.}}$$

$$I_1 = I_2 + I_{Bsat.}$$

$$I_1 = \frac{V_{cc} - V_{BE}}{R_c + R_1} = \frac{V_{BB} + V_{BE}}{R_2} + I_{Bsat.} \quad \text{—(1)}$$

$$I_{Bmin} = \frac{I_{csat.}}{\beta}$$

$I_{Bsat.} > I_{Bmin}$ (In order for the transistor Q_1 to be well in saturation)

assume $I_{Bsat.} = 2 * I_{Bmin}$.

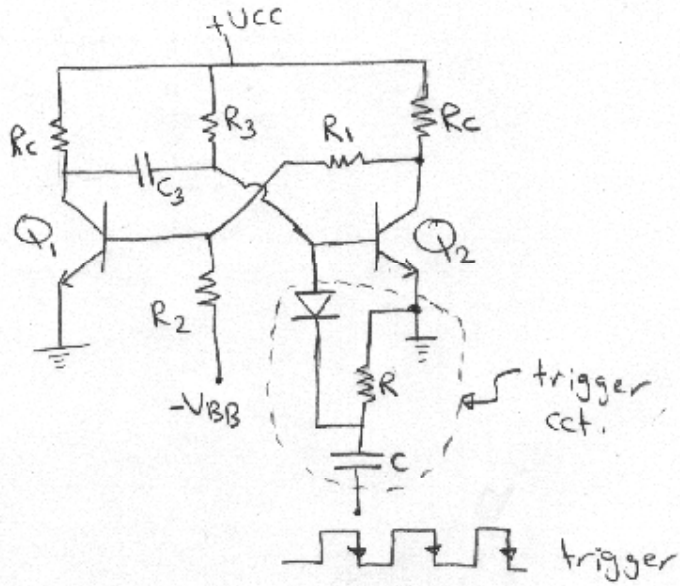
$$V_{B_2} = 0.2 * \frac{R_2}{R_1 + R_2} + (-V_{BB}) \frac{R_1}{R_1 + R_2} \quad \text{— (2)}$$

Assume $V_{B_2} = -1$ (In order for Q_2 to be off).

$$-1 = 0.2 * \frac{R_2}{R_1 + R_2} + (-V_{BB}) \frac{R_1}{R_1 + R_2}$$

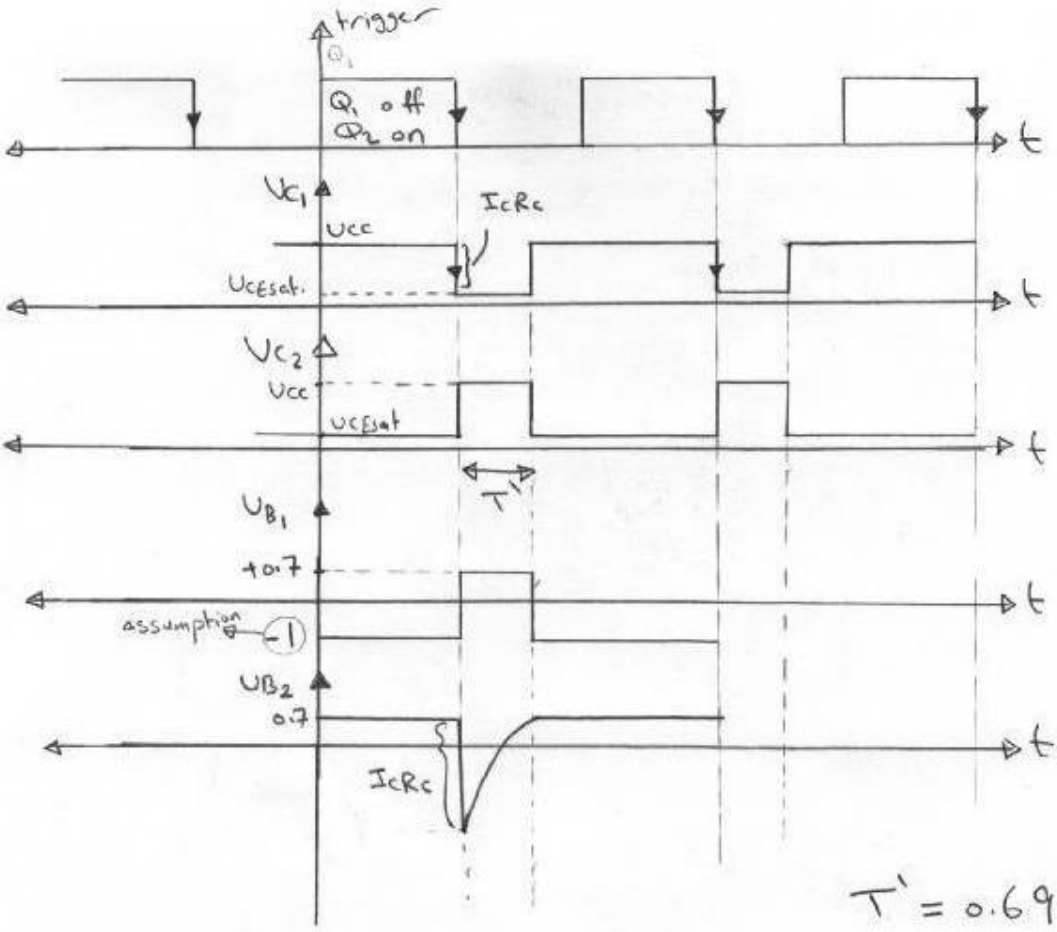
This multivibrator is designed such that one transistor is well into saturation and the other is well below cut off.

(2) Monostable Multivibrator:-



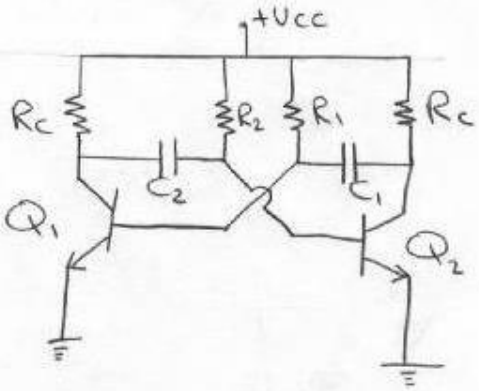
The monostable multivibrator has one stable and one quasi stable state, they happen when:-

(1) Q_1 off, Q_2 on (stable).
(2) Q_1 on, Q_2 off (quasistable).

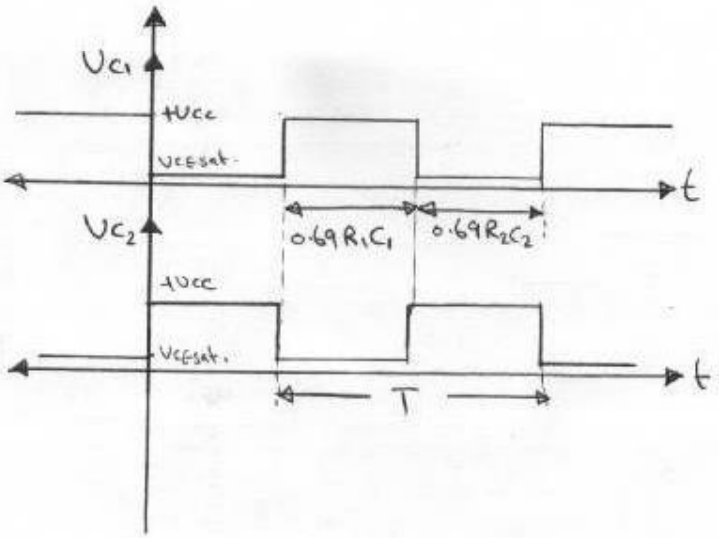


$$T' = 0.69 R_3 C_3$$

(3) Astable Multivibrator:-



This multivibrator has no stable states. The circuit operates as a free running oscillator without external trigger.



T = period of the pulse train.

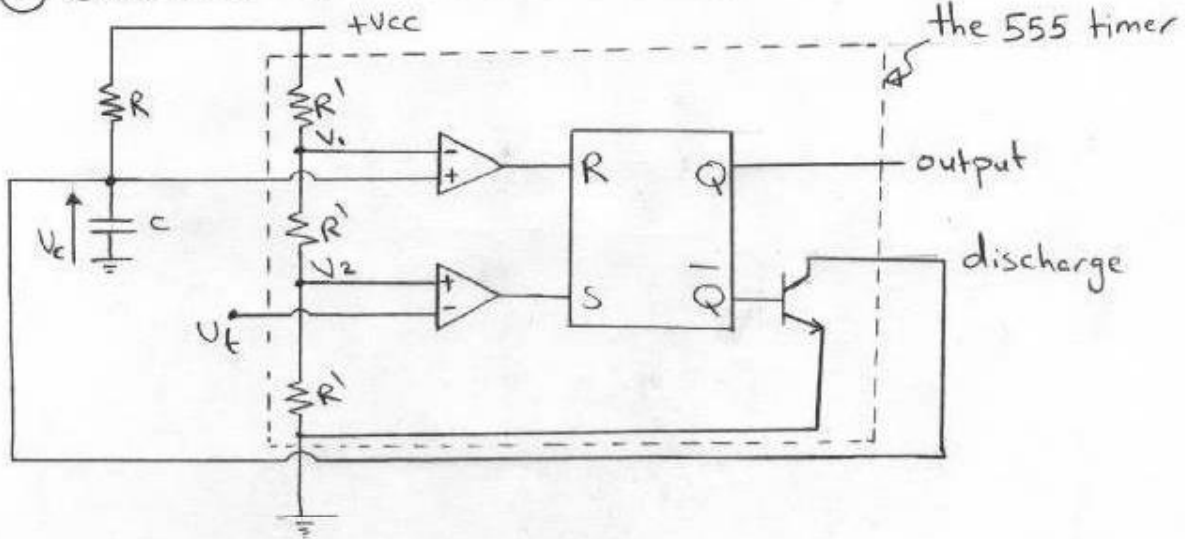
$T = 0.69 R_1C_1 + 0.69 R_2C_2$

if $R_1 = R_2 = R$ and $C_1 = C_2 = C$

then we have a square waveform generator with a period $T = 1.38\ RC$.

The 555 timer

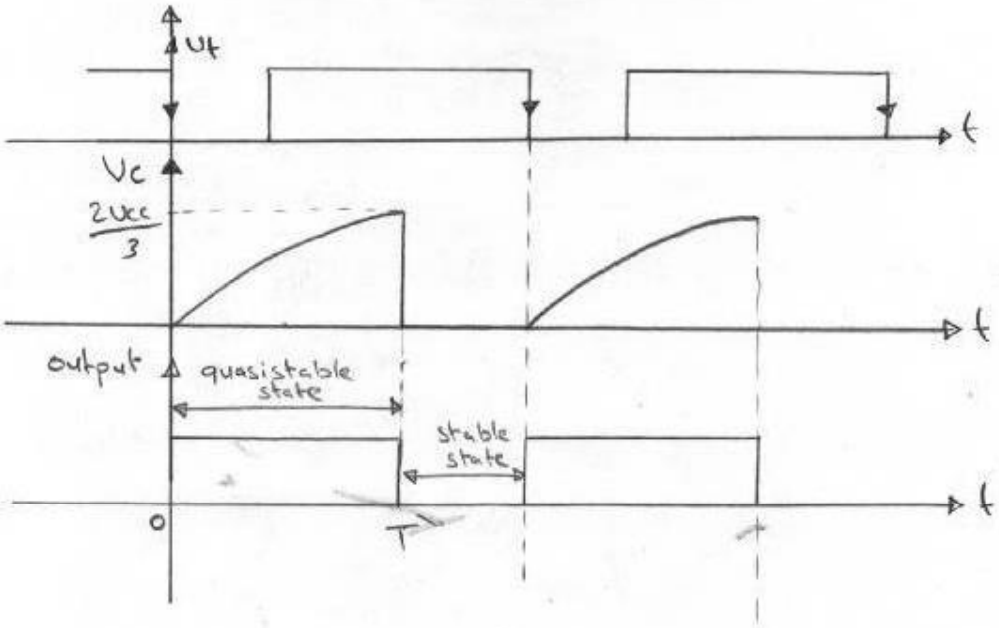
(a) Connected as a monostable cct.:-



$V_1 = \frac{2V_{cc}}{3}$, $V_2 = \frac{V_{cc}}{3}$

V_t :- trigger

$V_t > \frac{V_{cc}}{3}$

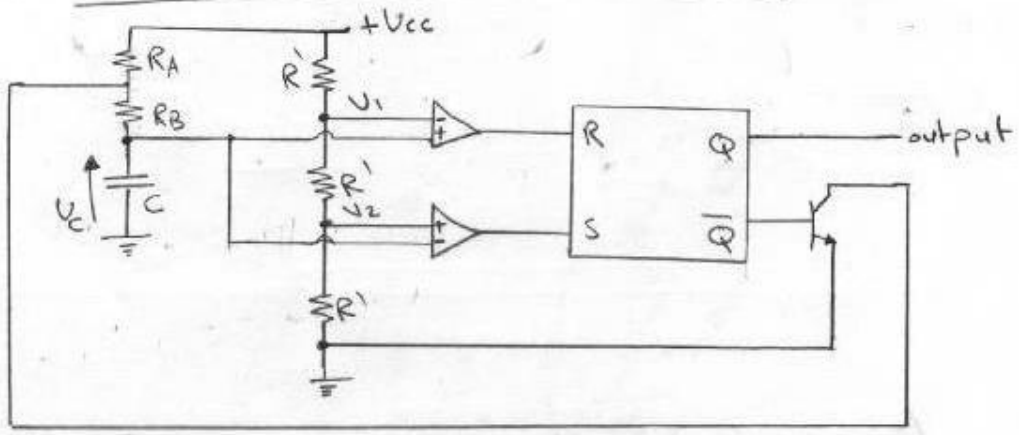


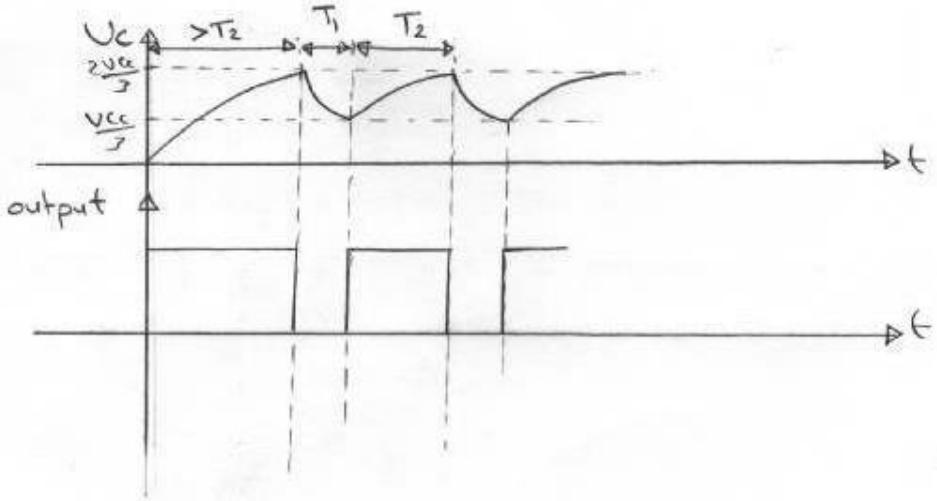
$$V_c = V_{cc}\left(1 - e^{-t/\tau}\right)$$

$$\frac{2V_{cc}}{3} = V_{cc}\left(1 - e^{-T'/RC}\right)$$

$$T' = (\ln 3)\,RC$$

(b) Connected as an astable cct. :-





$T = T_1 + T_2$

$f = \frac{1}{T}$

To find T_1 :-

$$V_c = \frac{2V_{cc}}{3} e^{-t/(R_B C)}$$

$$\frac{V_{cc}}{3} = \frac{2V_{cc}}{3} e^{-T_1/(R_B C)}$$

$$T_1 = [\ln 2] R_B C$$

To find T_2 :-

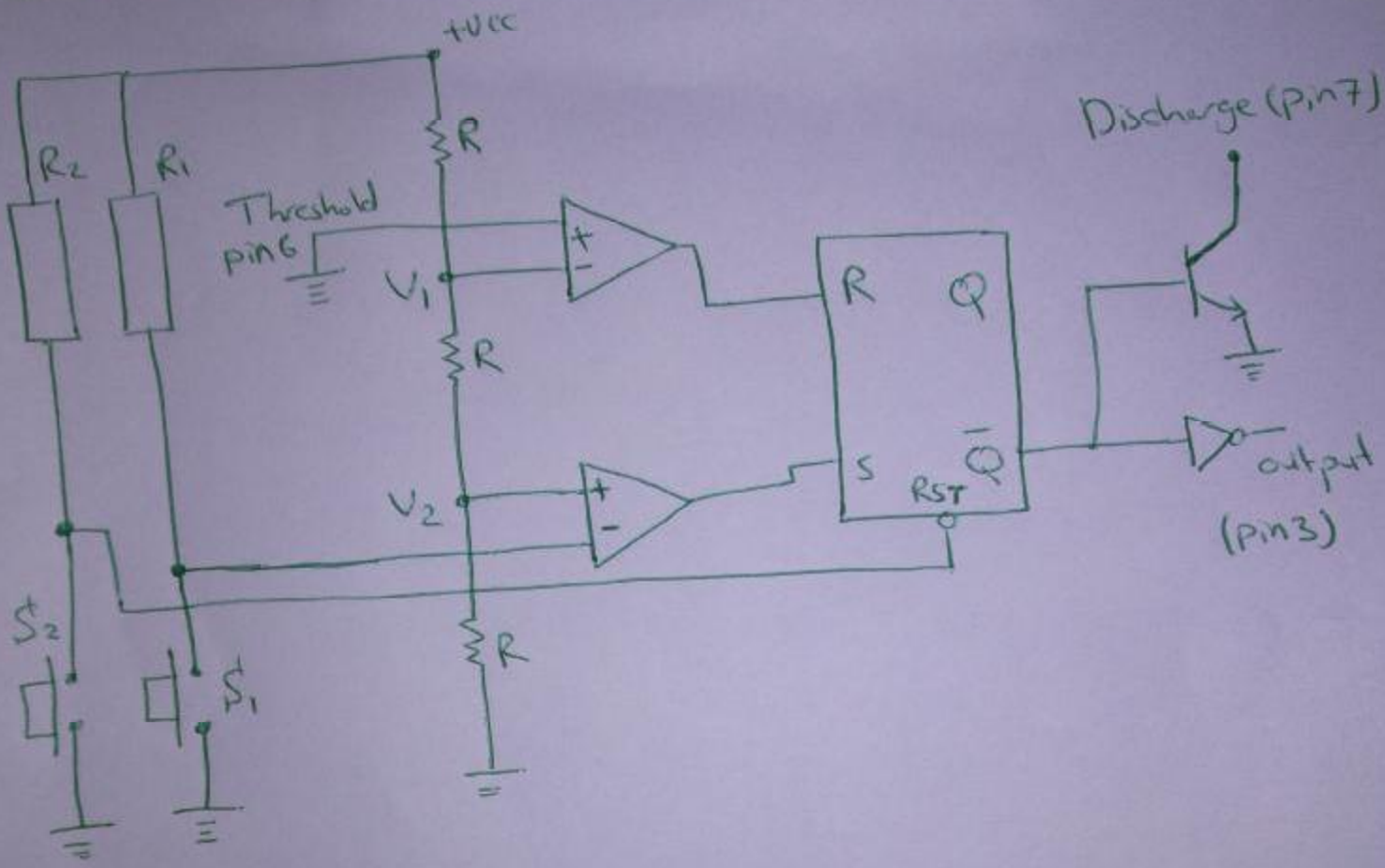
$$V_c = V_{cc} + \left(\frac{V_{cc}}{3} - V_{cc}\right) e^{-t/[(R_A+R_B)C]}$$

$$\frac{2V_{cc}}{3} = V_{cc} + \left(\frac{V_{cc}}{3} - V_{cc}\right) e^{-T_2/[(R_A+R_B)C]}$$

$$T_2 = [\ln 2] (R_A + R_B) C$$

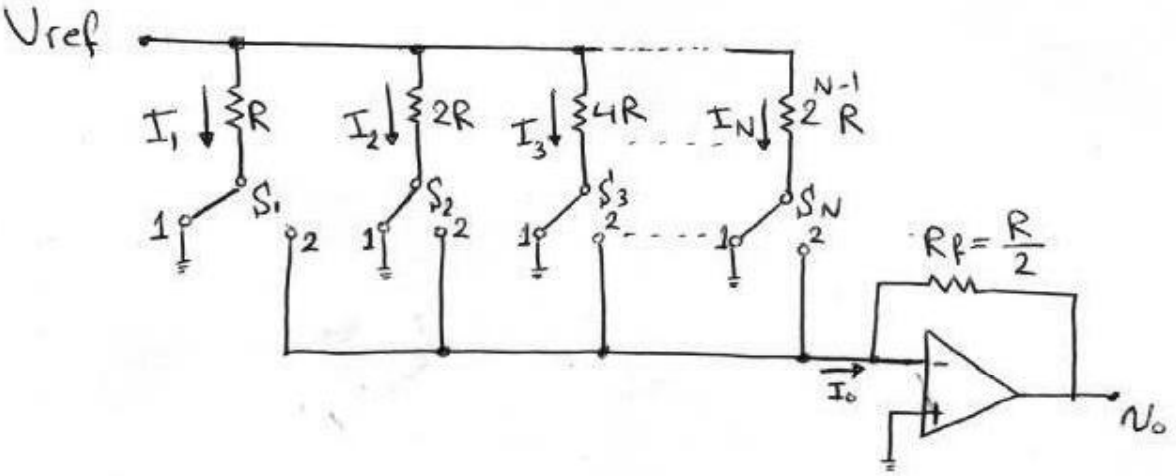
$$T = (\ln 2) C (2R_B + R_A), \quad \text{Duty cycle} = \frac{R_A + R_B}{R_A + 2R_B}$$

③ The 555 Timer as a Bistable Multivibrator



Digital-to-Analog (D/A) converters:-

① Binary-weighted Resistor D/A Converter:-



An N-bit D/A converter using binary weighted resistors

* The switches are controlled by an N-bit digital input, $(b_1, b_2, \ldots, b_N)$.
* b_i is either 0 or 1.
* b_N is the least significant bit (LSB) and b_1 is the Most " " " (MSB).

* if $b_i = 1$ the switch is at position (2)
  if $b_i = 0$ the switch is at position (1)

$$I_o = I_1 b_1 + I_2 b_2 + I_3 b_3 + \cdots + I_N b_N .$$

$$= \frac{V_{ref}}{R} b_1 + \frac{V_{ref}}{2R} b_2 + \frac{V_{ref}}{4R} b_3 + \cdots + \frac{V_{ref}}{2^{N-1} R} b_N .$$

$$D = \frac{b_1}{2^1} + \frac{b_2}{2^2} + \frac{b_3}{2^3} + \cdots + \frac{b_N}{2^N}$$

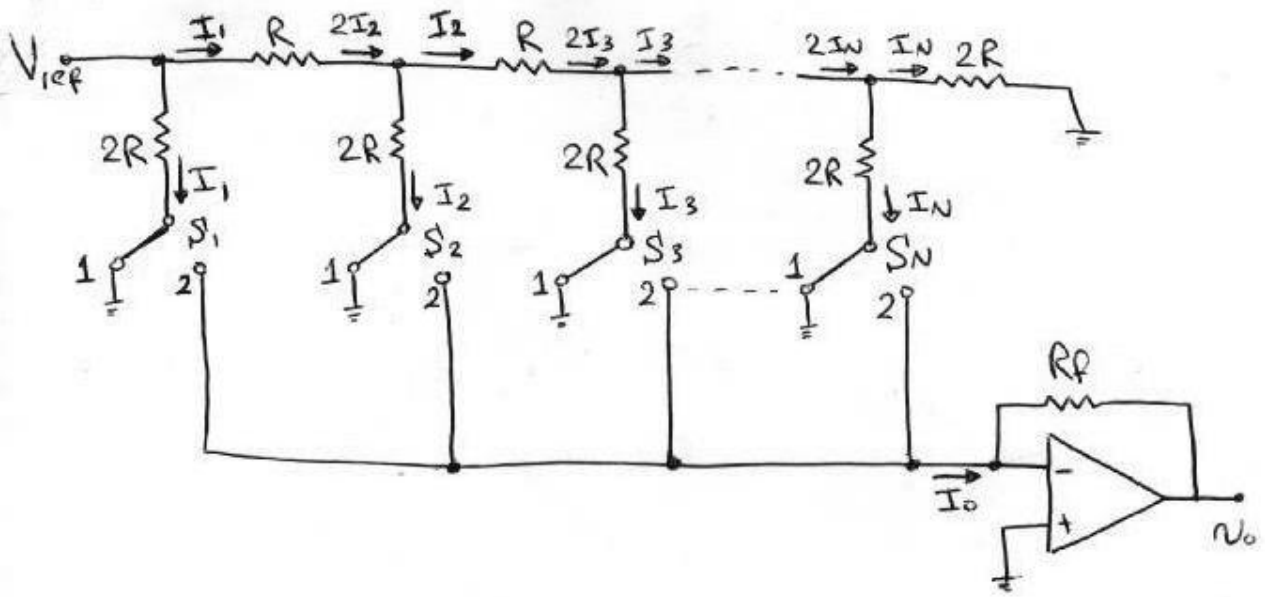
$$I_o = \frac{2 V_{ref}}{R} D$$

$$V_o = -I_o R_f = -V_{ref} D .$$

so that the output V_o is directly proportional to the digital input signal.

* a disadvantage of Binary weighted Resistor D/A converter is that when $N > 4$ there will be a difficulty in maintaining accuracy of resistor values.

② The R-2R Ladder D/A



$$I_o = I_1 b_1 + I_2 b_2 + \cdots + I_N b_N$$

$$I_1 = 2I_2 = 4I_3 = \cdots = 2^{N-1} I_N$$

$$I_1 = \frac{V_{ref}}{2R}$$

$$I_o = \frac{V_{ref}}{R}\left(\frac{b_1}{2^1} + \frac{b_2}{2^2} + \cdots + \frac{b_N}{2^N}\right)$$

$$\therefore I_o = \frac{V_{ref}}{R} D$$

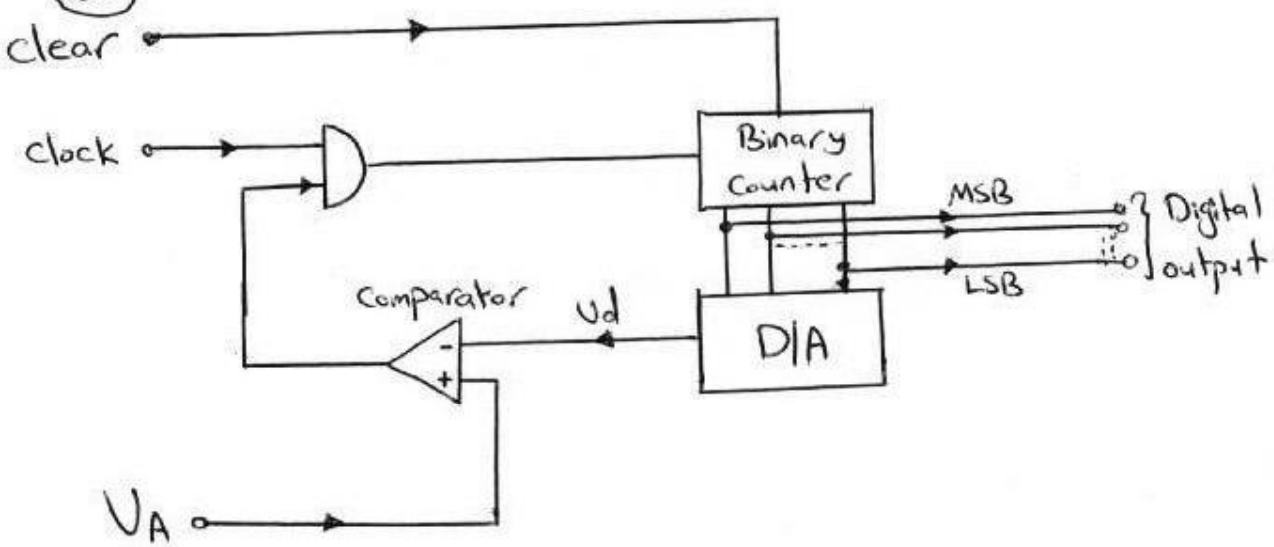
$$V_o = -I_o * R_f$$

$$= -V_{ref} * D \quad \text{if } (R_f = R)$$

Analog-to-Digital (A/D) converters:-

(1) The Counting A/D converter:-

(a)



* The clear pulse resets the counter.
* The counter will then count the number of clock pulses.
* This count will be converted into Analog by (D/A).
* If this count is still less than Va the counter continues untill the counter reaches the value of VA.
* At that point the AND gate is disabled and the counting stops.

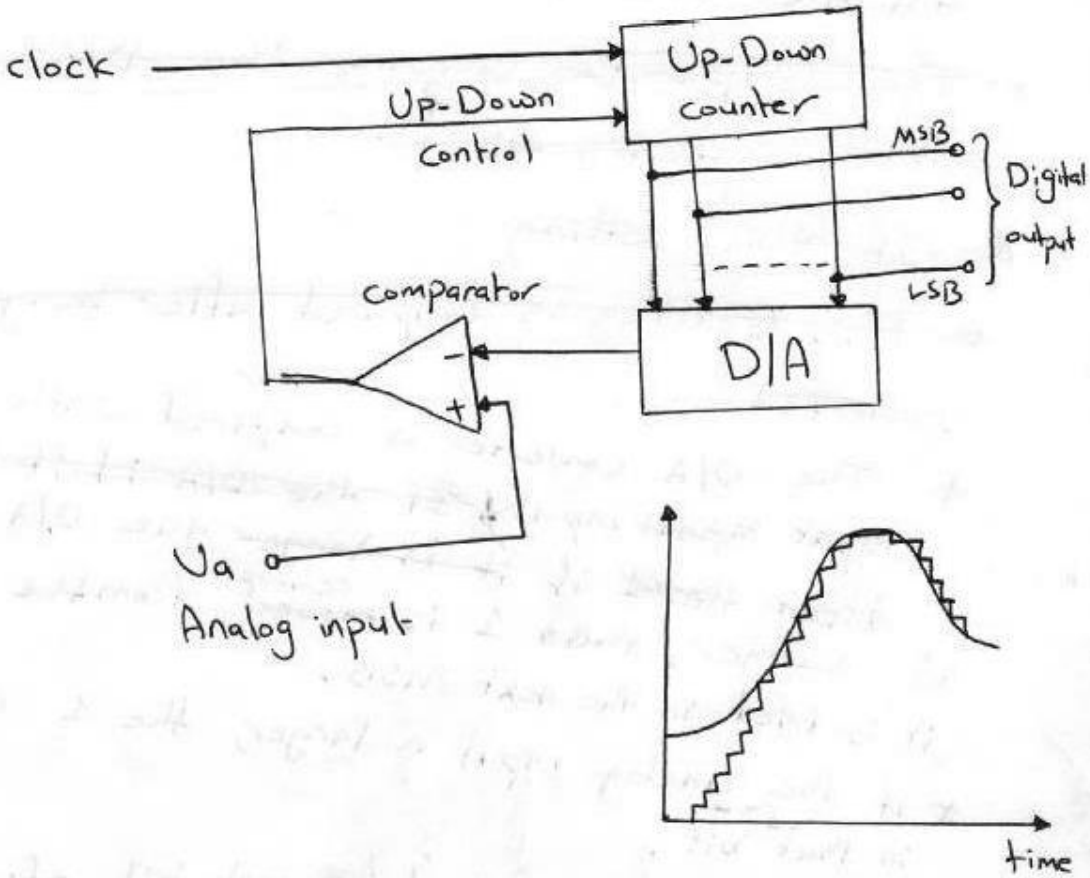
* The counter reading represents the analog input

* If Va is varying with time then a sample and hold circuit is required. The minimum interval between samples is to be nT seconds, where

n = is the number of clock pulses for the maximum value of the analog voltage.

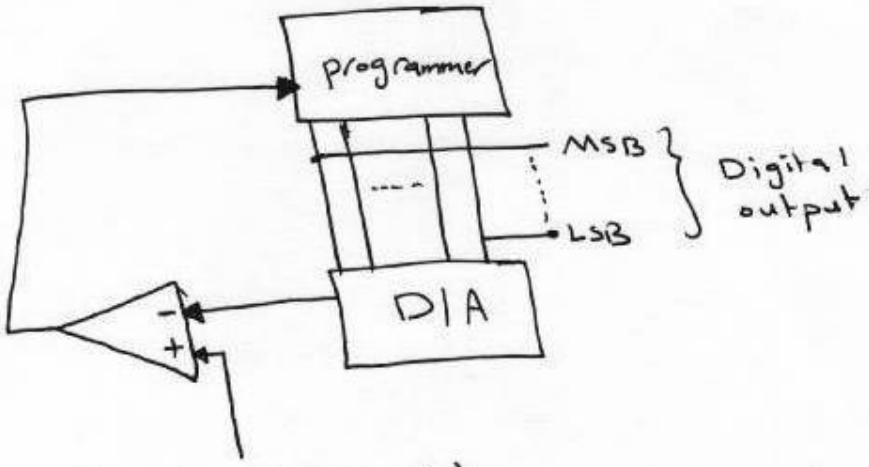
T = is the clock period.

(b) Tracking or Servo counting A/D converter:-



The Conversion time is small for small changes in the sampled analog signal and hence this system can be used effectively as a tracking A/D Converter.

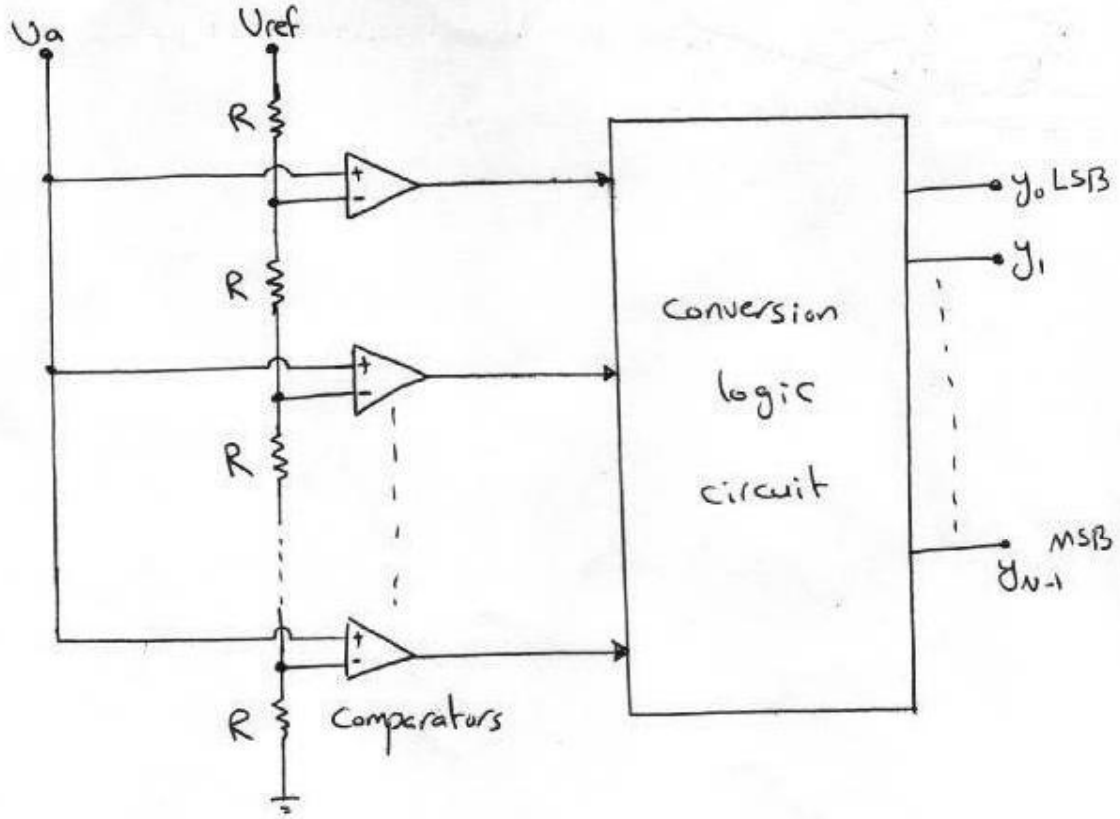
(2) The Successive - Approximation A/D Converter



* The programmer sets the MSB to 1 with all other bits to 0.
* The D/A Converter output is Compared with the analog input, if the D/A output is larger, the 1 is removed from the MSB, and it is tried in the next MSB.
* if the analog input is larger, the 1 remains in that b
* Thus a 1 is tried in each bit of the D/A Converter until the binary equivalent of the analog Signal is obtained at the end of the process.

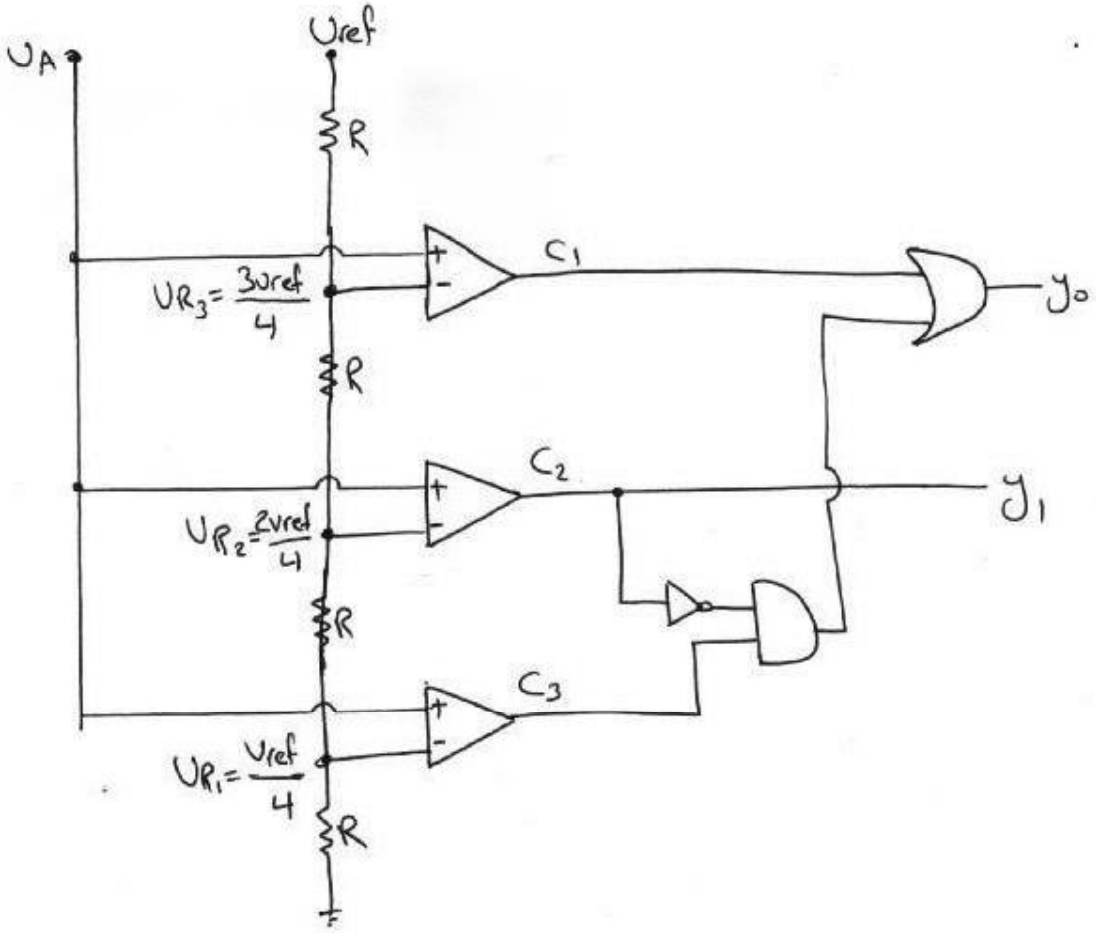
* For an N-bit system, the conversion time is N clock periods as opposed to a worst case of 2^N clock periods for the counting-type A/D converter.

(2) The Simultaneous, parallel or Flash A/D converter :-



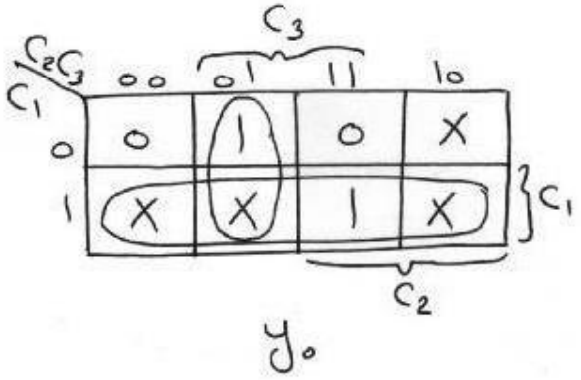
This converter is the fastest of all converters.

for example if $N=2$ then 3 comparators are required where Va is applied to them simultaneously and compared with equally spaced thresholds as in the following:-



* a disadvantage of this technique is the complexity of hardware. The number of comparators needed is $2^N - 1$ where N is number of output bits.

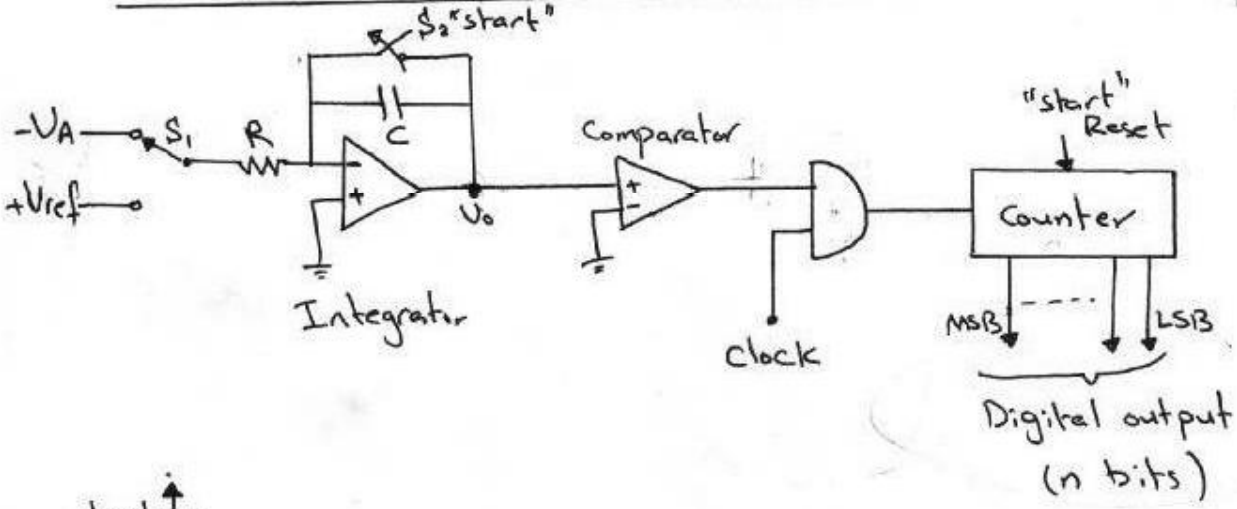
Va	C_3	C_2	C_1	y_1	y_0
$0 < Va < \frac{Vref}{4}$	0	0	0	0	0
$\frac{Vref}{4} < Va < \frac{2Vref}{4}$	1	0	0	0	1
$\frac{2Vref}{4} < Va < \frac{3Vref}{4}$	1	1	0	1	0
$\frac{3Vref}{4} < Va < Vref$	1	1	1	1	1

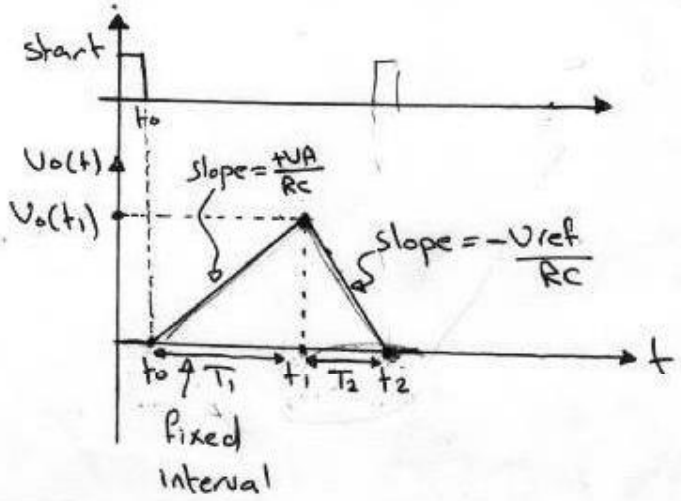


$$Y_1 = C_2$$

$$Y_0 = C_1 + C_3\overline{C_2}$$

(14) Integrating Dual-Slope A/D Converter:-





$$V_o(t_1) = \frac{-1}{RC}\int_{t_o}^{t_1} (-V_A)\, dt = \frac{V_A}{RC}(t_1 - t_o)$$

$N_1 = 2^n$

$T_1 = (t_1 - t_o) = N_1 T$, T = clock period.

$f_c = \frac{1}{T}$, f_c: clock frequency

$\therefore V_o(t_1) = \frac{V_A}{RC} \cdot N_1 T$

$$V_o(t_2) = V_o(t_1) + \frac{-1}{RC}\int_{t_1}^{t_2} V_{ref}\, dt$$

$$0 = V_o(t_1) + \frac{-1}{RC}\int_{t_1}^{t_2} V_{ref}\, dt .$$

$$\frac{V_A}{RC} \cdot N_1 T = \frac{V_{ref}}{RC}(t_2 - t_1)$$

$T_2 = t_2 - t_1 = N_2 T$

$\therefore \frac{V_A}{RC} \cdot N_1 T = \frac{V_{ref}}{RC} \cdot N_2 T$

$N_2 = \frac{N_1}{V_{ref}} V_A$

$\boxed{N_2 = k(V_A)}$, where $K = \frac{N_1}{V_{ref}}$

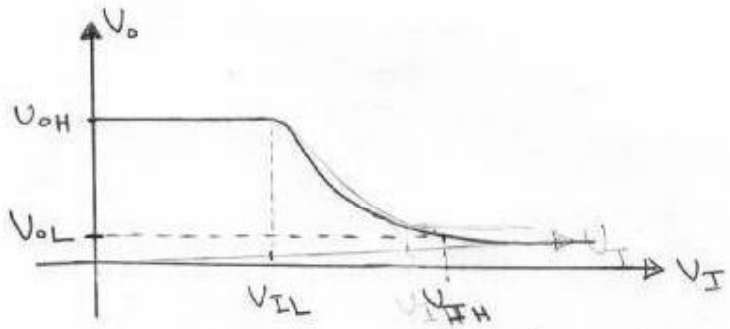
This converter is very accurate but very slow.

Logic families

Logic circuit characterization:-

The following parameters are used to characterize the operation and performance of a logic-circuit family.

(a) Noise Margins:-

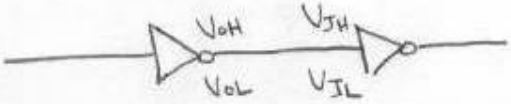


Typical voltage transfer c/c's (VTC) of a logic inverter

* The V_{IL} is the maximum value that the input can have while being interpreted by the inverter as representing a logic (0).

* The V_{IH} is the maximum value that V_I can have while being interpreted by the inverter as representing logic (1).

for example:-



$N_{MH} = V_{OH} - V_{IH}$

$N_{ML} = V_{IL} - V_{OL}$

* The robustness of the logic cct. family is defined by its ability to reject noise and thus by its noise margins (NM_H , NM_L).

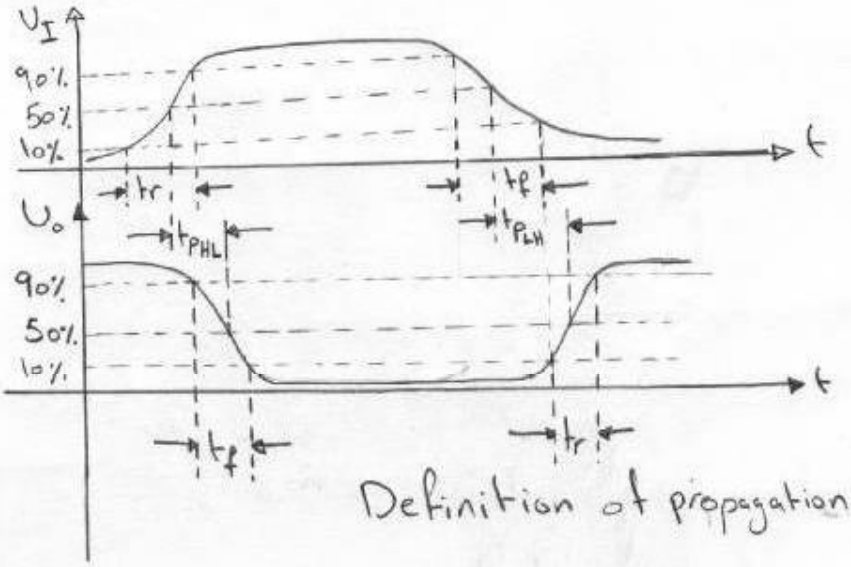
(b) power dissipation

There are two types of power in a logic gate, static and Dynamic.

static power dissipation :- is the power the gate dissipate in the absence of switching action. It results from the presence of a path between the power supply and ground in one or both of its two state. (i.e. with the o/p either low or high).

Dynamic power dissipation :- Occures only when the gate is switched due to the presence of a capacitor between the o/p node and ground.

(c) propagation delay :-



Definition of propagation delay

t_r : the rise time.

t_f :- the fall time.

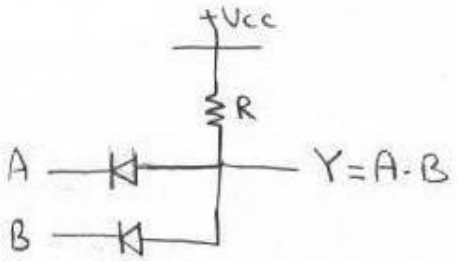
t_{PHL} :- High-to-Low propagation delay.

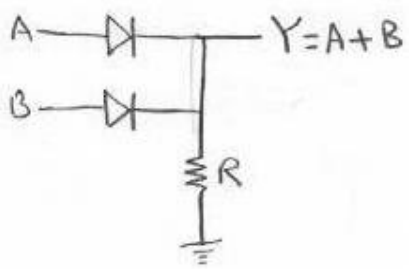
t_{PLH} :- Low-to-High propagation delay.

(d) Fan out:-

The fan out is the maximum number of similar gates that a gate can drive while remaining within gauranteed specifications.

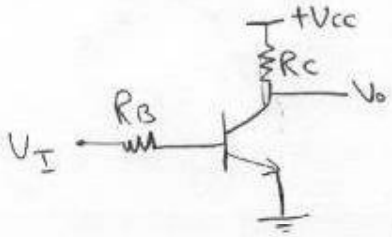
(1) Diode Logic family





The BJT Digital Circuits:-

Basic BJT Inverter:-



Example:-

Draw the VTC of the basic BJT inverter if $R_B = 10K\Omega$, $R_C = 1K\Omega$, $\beta_F = 50$ and $V_{CC} = 5V$.

Solution:-

(1) if the i/p equals a low voltage

$V_I = V_{oL} = V(o) = 0.2V = V_{CEsat.}$

$V_o = V_{oH} = V_{CC} = 5V.$

(2) At $V_I = V_{IL}$, the transistor begins to turn on, then

$V_{IL} = 0.7V.$

(3) if $V_{IL} < V_I < V_{IH}$

the transistor is in the active region having again of

$$A_V = \frac{-\beta_o R_C}{R_B + r_\pi}$$

(4) $$I_{Bmin} = \frac{I_{csat.}}{\beta_F}$$

$$I_{csat.} = \frac{V_{CC} - V_{CEsat.}}{R_C}$$

$V_{IH} = I_{Bmin} * R_B + 0.7 \Rightarrow$ from the i/p loop.

$= 1.66V$

(5) $V_I = V_{oH} = V_{CC} = 5V$

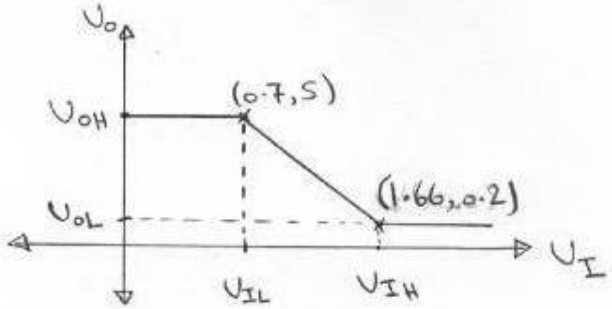
$$I_{csat.} = \frac{V_{CC} - V_{CEsat.}}{R_C}$$

$$I_{Bsat.} = \frac{V_{oH} - 0.7}{R_B}$$

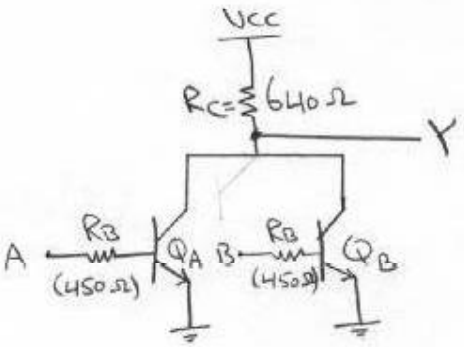
$$\beta_{forced} = \frac{I_{csat.}}{I_{Bsat.}} = 1.1$$

⑥ $N_{MH} = V_{OH} - V_{IH} = 3.34\,V$

$N_{ML} = V_{IL} - V_{OL} = 0.5\,V.$



Resistor Transistor Logic (RTL)



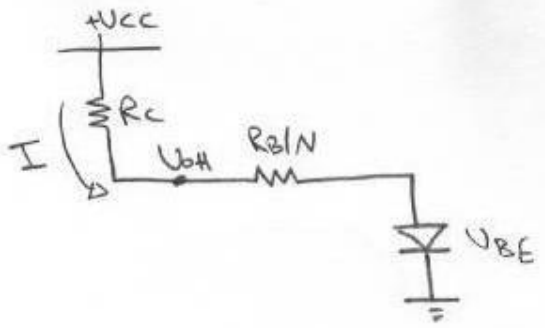
A two input NOR gate of the RTL family

$Y = \bar{A} \cdot \bar{B} = \overline{A+B}$

* The noise margins of the RTL gate are narrow because the V_{OH} is lowered when driving other similar gates.
* The RTL gate dissipate a large amount of power (12 mw).

Example:- An RTL gate is driving N similar gates, find an expression for V_{OH} in terms of N and then find the value of V_{OH}, if $N = 5$.

Solution:-

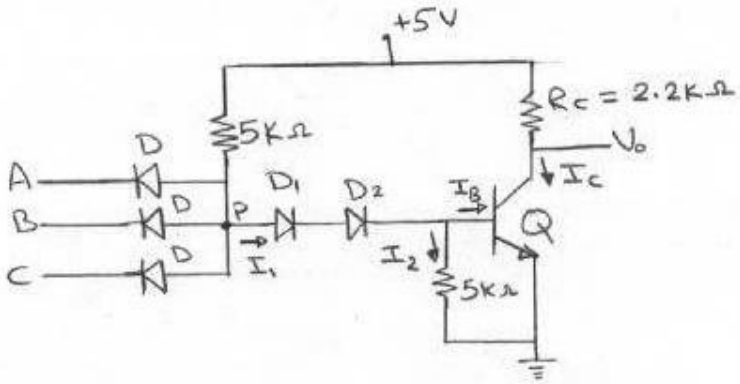


$$V_{oH} = V_{cc} - R_c \frac{V_{cc} - V_{BE}}{R_c + \frac{R_B}{N}}$$

if $V_{cc} = 3V$, $N = 5$

$V_{oH} = 1V$

Diode Transistor Logic (DTL) family:-



DTL NAND gate

Example:-

For the DTL NAND gate above, assume that $V_{BEsat} = 0.7V$, $V_\gamma = 0.5V$, and $V_{CEsat.} = 0.2V$. The drop across a conducting diode is 0.7V and V_γ(diode) = 0.6V (A) Verify that the cct. functions as a NAND gate for $\beta_F > \beta_{fmin}$ (assume that Q is unloaded by a following gate).

(B) Calculate β_{fmin}.

(C) Will the circuit operate properly if D_2 is not used.

Solution:-

logic (0) = V_{CEsat} = 0.2V.

logic (1) = V_{cc} = 5V.

(A)

* if at least one input is low its diode conducts and V_p = 0.2 + 0.7 = 0.9 V. D_1 and D_2 are not conducting since 3*0.7 = 2.1 V is required and V_{BE} = 0V.

Since V_γ of Q = 0.5V then Q is off :-

∴ Y = V_{cc} = 5V = logic (1).

* Now, if all inputs are high at V(1) = V_{cc} = 5V.

Assume all input diodes are off, that D_1 and D_2 conduct and that Q is in saturation.

So V_p = 0.7 + 0.7 + 0.7 = 2.1V.

then each input diode (D) will have a voltage of 2.1V on its anode and 5V on its cathode, thus justifying the assumption that D is off.

$$I_1 = \frac{5 - 2.1}{5k} = 0.58\,mA.$$

$$I_2 = \frac{0.7}{5k} = 0.14\,mA.$$

$$I_B = I_1 - I_2 = 0.44\,mA.$$

Assuming that $\beta_F > \beta_{fmin}$, this value of I_B saturates Q and makes $V_o = V(0) = V_{CEsat}$. So we have verified the NAND gate.

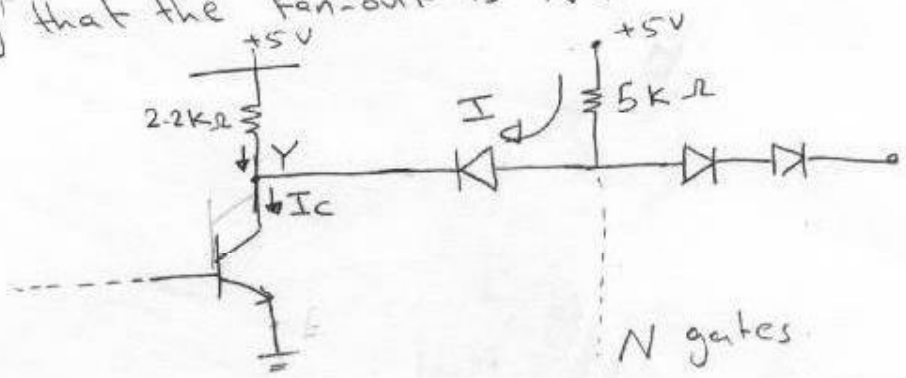
(b) $I_{csat.} = \frac{5 - 0.2}{2.2} = 2.182\,mA$

$\beta_{f\,min} = \frac{I_{csat.}}{I_B} = \frac{2.182}{0.44} = 4.96$

Thus for $\beta_F \geq 4.96$, the assumption of Q is saturated is valid.

(c) If at least one input is at V(0), then $V_p = 0.2 + 0.7 = 0.9V$. Hence if only one diode D_1 is used between p and the base B, then $V_{BE} = 0.9 - 0.6 = 0.3V$, where 0.6V is the diode cut-in voltage. Since the transistor cut-in voltage is $V_\gamma = 0.5V$, theoretically Q is cut-off. However, this is not a very conservative design because a small (>0.2V) spike of noise will turn Q on.

If the DTL gate is driving N similar gates, we say that the fan-out is N :-



when $Y = V(o) = 0.2V$, the input current I. of a following stage adds to the collector current of Q.

Assume all the inputs to the diodes of the following stages are high except the ones driven by Q.

then $I = \frac{5-0.9}{5} = 0.82mA$.

total I_C of Q $= 0.82 \cdot N + 2.182 mA$

I_B the same as before loading $= 0.44mA$ and assume a reasonable value of $\beta_{min} = 30$

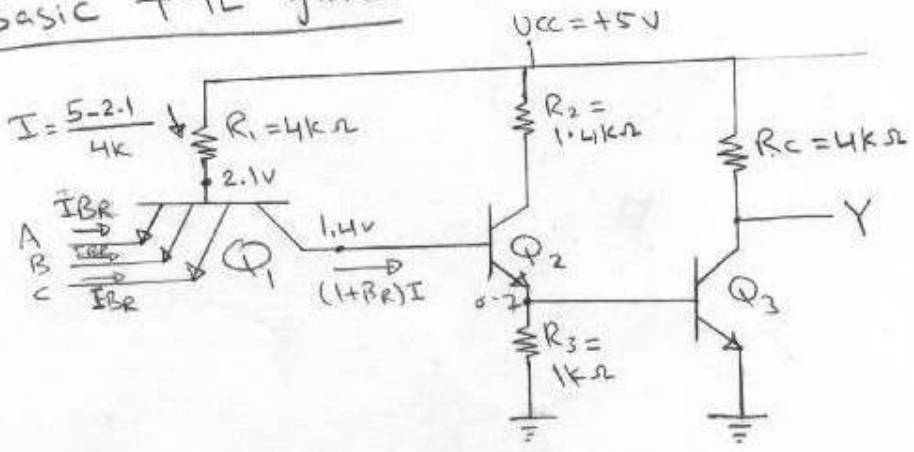
$I_C = \beta_{f\,min} I_B$

$I_C = 0.82N + 2.182 = 30 * 0.144 = 13.2mA$.

$N = 13.436$, N must be an integer then $N = 13$. of course the current rating of Q must not be exceeded.

Transistor - Transistor Logic (TTL, T^2L):-

(a) Basic TTL gate:-

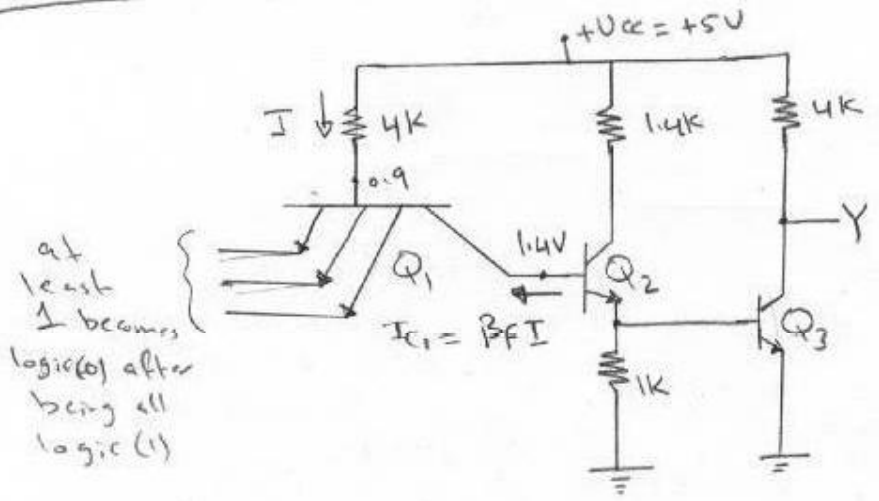


TTL - NAND gate (when all inputs are high)

Case I :- when all inputs are high = logic (1)

* The emitters of Q_1 are reverse biased.
* The collector/Base junction of Q_1 is forward biased.
* Q_1 is operating in the inverted active mode.
* β_R (reverse β) is very small. ($\beta_R = 0.2$)
* $(\beta_R + 1) I$ is a sufficient current to drive Q_2 and Q_3 into saturation and the output Y equals to logic (0) = 0.2V.

Case II :- If at least one of the inputs is V (0).



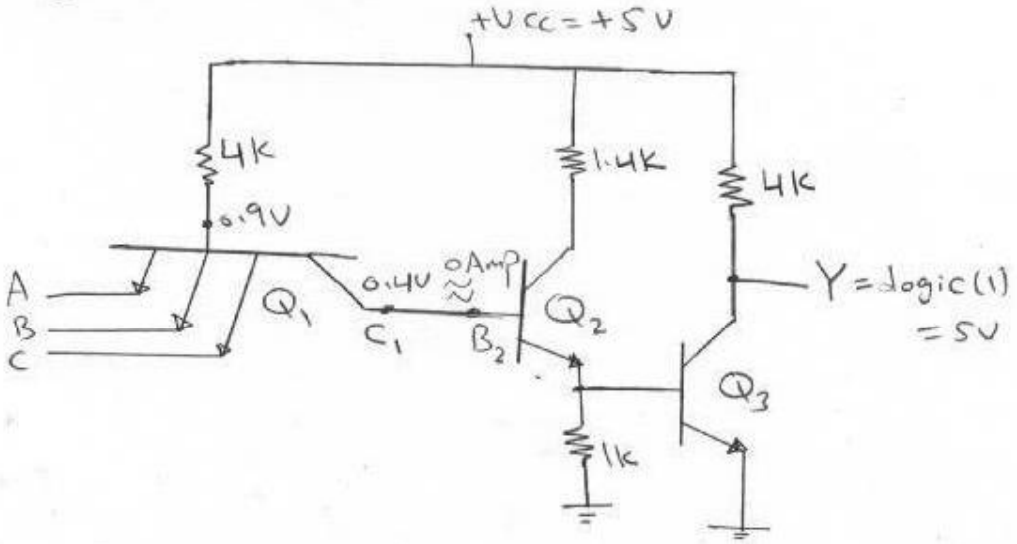
when Q_2 and Q_3 are still momentairily ON (saturated).

* The current I will be diverted to the emitters of Q_1.
* The base/emitter junction of Q_1 is forward biased.
* V_B of Q_1 = 0.9V.
* Q_1 is operating momentairily in the normal active mode.
* $I_{C_1} = \beta_F I$ which is a large current that will turn Q_2 and Q_3 off.

* when Q_2 is off I_{B_2} is a small current (in nanoamperes), so $I_{B_1} > \frac{I_{C_1}}{\beta}$ and Q_1 will saturate.

* V_{C_1} equals $0.2 + 0.2 = 0.4V$, which is a small voltage that will keep Q_2 and Q_3 off.

Y = logic (1) = $V_{cc} = 5V$.



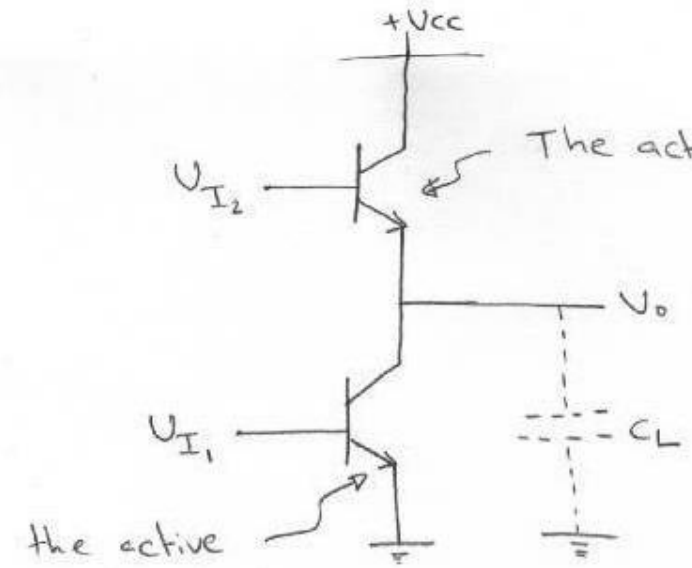
when Q_2 and Q_3 are off.

Output Circuit of TTL:-

* The C.E o/p stage provides fast discharging of a load capacitance but rather slow charging.

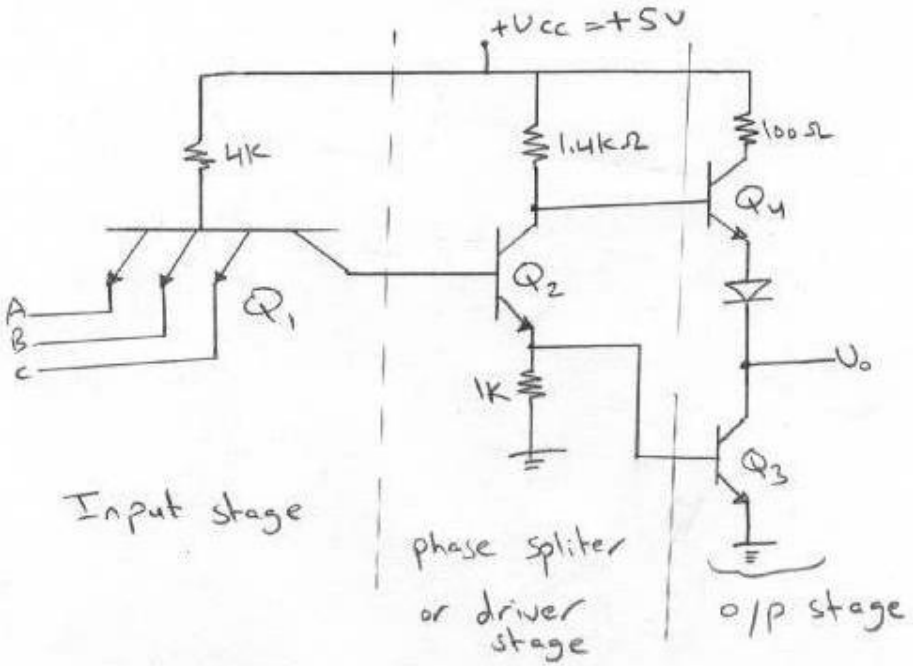
* while the opposite is obtained in the C.C output stage, it provides fast charging of the load capacitance, but slow discharge of C_L.

An optimum output stage will be the totem-pole output stage as shown:-

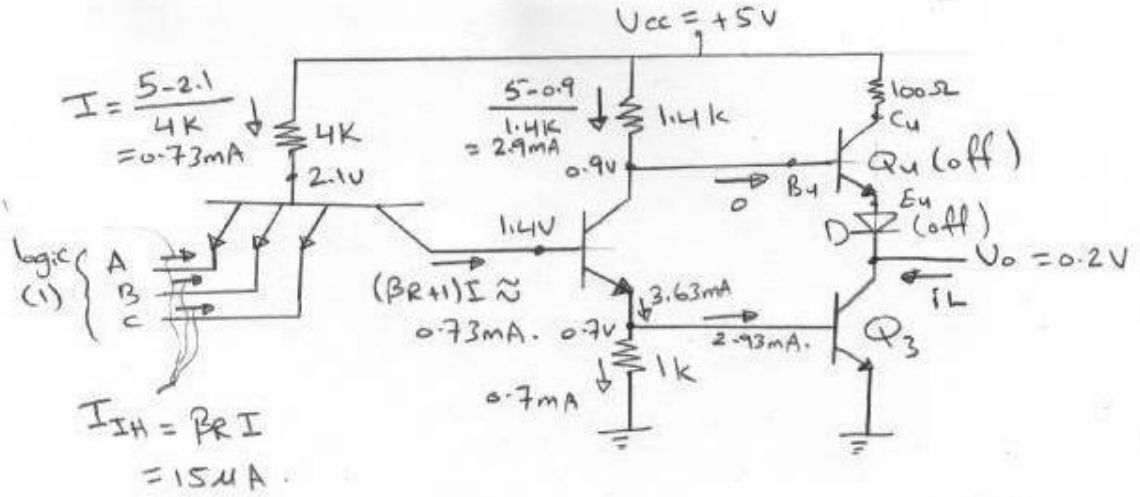


V_{I_1} and V_{I_2} are complementary inputs.

(b) TTL with totem-pole output:-



Case I:- when all inputs are high



* when the input is high both Q_2 and Q_3 are driven into saturation, So $V_o = V_{CEsat.} = 0.2V$.

Q_u should be off which is obtained by adding Diode D.

* if D does not exist then:-

$$V_{C_2} = V_{CE_2}{}_{sat.} + V_{BE_3}{}_{sat.} = 0.2 + 0.7 = 0.9V.$$

$$V_{BE_u} = V_{B_u} - V_{CE_3 sat.} = 0.9 - 0.2 = 0.7V.$$

which will turn Q_u ON. and

$$I_{C_u} = \frac{V_{cc} - V_{CE_u(sat.)} - V_{CE_3(sat.)}}{100} = \frac{5 - 0.2 - 0.2}{100}$$

$$= 46mA \text{ (excessive and wasted current).}$$

therefore D was added so that

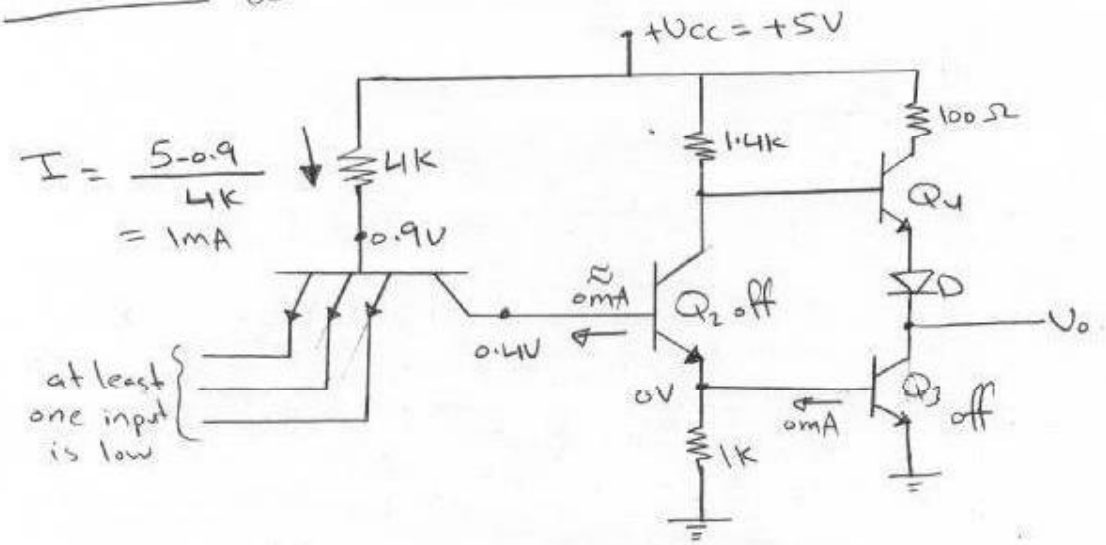
$$V_D + V_{BE_u} = V_{B_u} - V_{CE_3 sat.} = 0.7V$$

$\therefore$ Q_u and D are off since both of them require

1.4V to start conducting.

* In the low output state, the gate can sink a load current (i_L), provided that the value of i_L doesn't exceed $\beta * 2.93mA$ which is the maximum collector current that Q_3 can sustain while remaining in saturation.

Case II when at least one input is low.



Assume that V_o = logic(0) = 0.2V and one of the inputs becomes low.

V_o across C_L (load capacitance) remains momentairily at 0.2V.

Now Q_4 is in saturation and D is conducting,

$$V_{B4} = V_{BE4(sat.)} + V_D + V_o = 0.7 + 0.7 + 0.2 = 1.6V.$$

$$I_{B4} = \frac{V_{cc} - V_{B4}}{1.4K} = \frac{5 - 1.6}{1.4K} = 2.43mA$$

$$I_{C4} = \frac{V_{CC} - V_{CE4} - V_D - V_o}{0.1k} = \frac{5 - 0.2 - 0.7 - 0.2}{0.1} = 39mA$$

$$\beta_{fmin} = \frac{I_{C4}}{I_{B4}} = 16.05$$

Choose $\beta_F > 16.05$ then Q_4 is in saturation. As long as Q_4 is in saturation, the output voltage rises exponentially towards V_{CC} with a very small time constant. The final value of the output voltage is:-

$$V_o = V_{CC} - V_{BE4}(cutin) - V_D(cutin)$$
$$= 5 - 0.5 - 0.6 = 3.9V = logic(1)$$

TTL family with improved performance:-

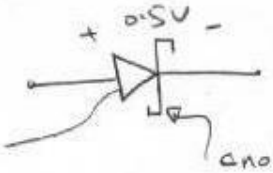
The TTL family is available in series emphasizing either high speed, low power, or both. These gates differ from one another in the numerical values of their resistors and in that some use Schottky transistors.

TTL series

Symbol	meaning
S	Schottky, high speed
LS	schottky, low power
–	standard (the previous one which have been studied)

There is the 74 series (0–70°C) and the 54 series (-55 – 125°C).

Schottky TTL (74S)%-

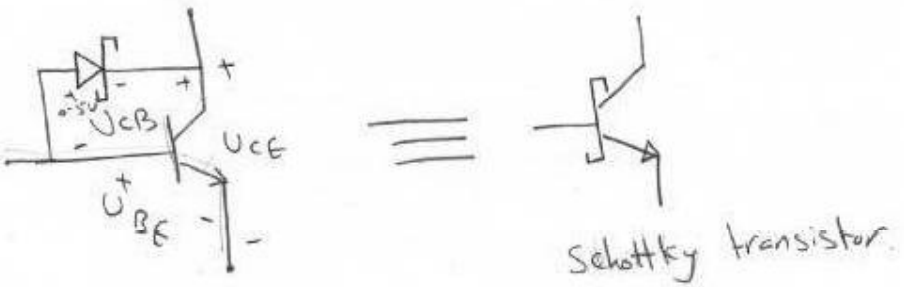


Cathode (metal)

anode (n-type semiconductor)

Schottky diode

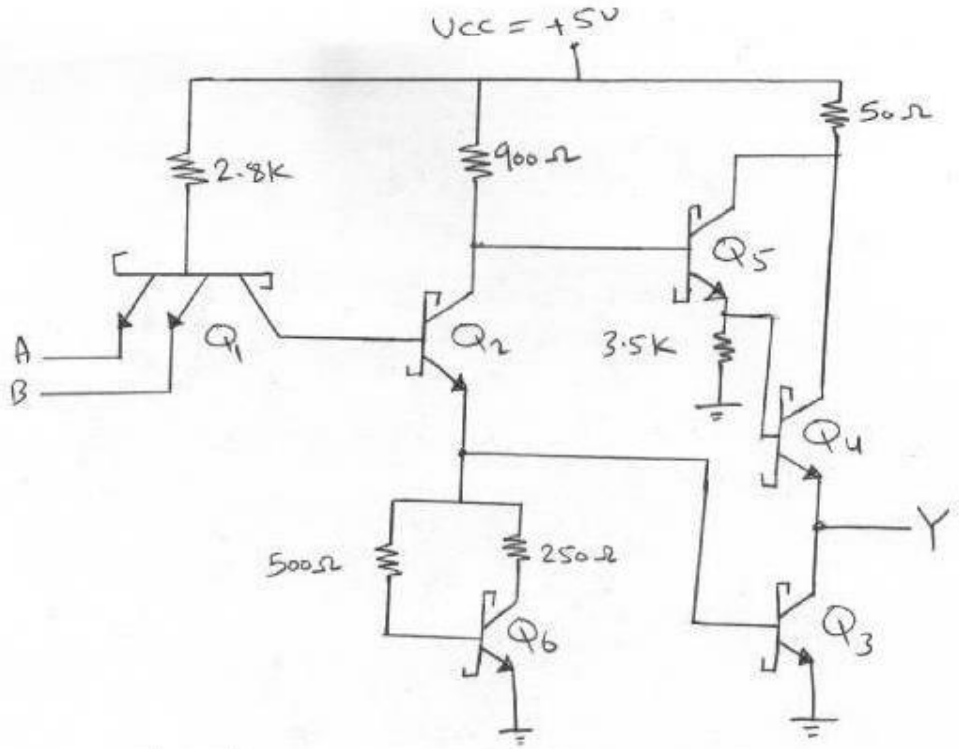
* The schottky diode is formed by bringing metal into contact with a moderately doped n-type semiconductor material.
* The forward voltage drop of the schottky diiode is 0.5V.



Schottky transistor

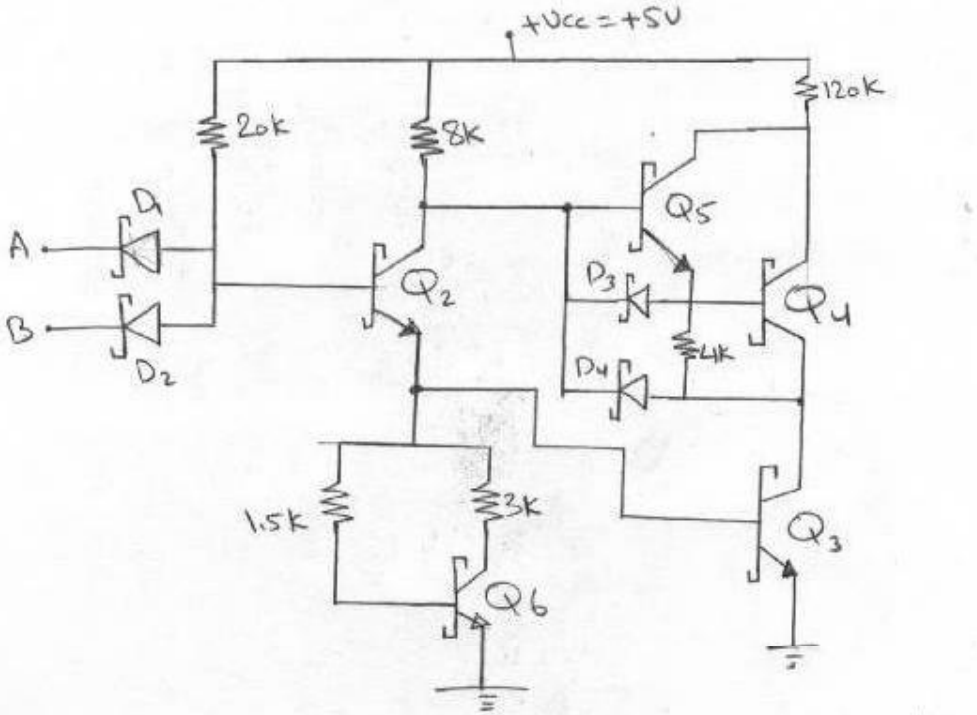
$V_{CE} = 0.7 - 0.5 = 0.2V$

* In schottky TTL, transistors are prevented from saturation by connecting a schottky diode between base and collector of the transistor as shown above.
* By avoiding saturation, the schottky transistor exhibits a very short turn off time.



Schottky TTL NAND gate.

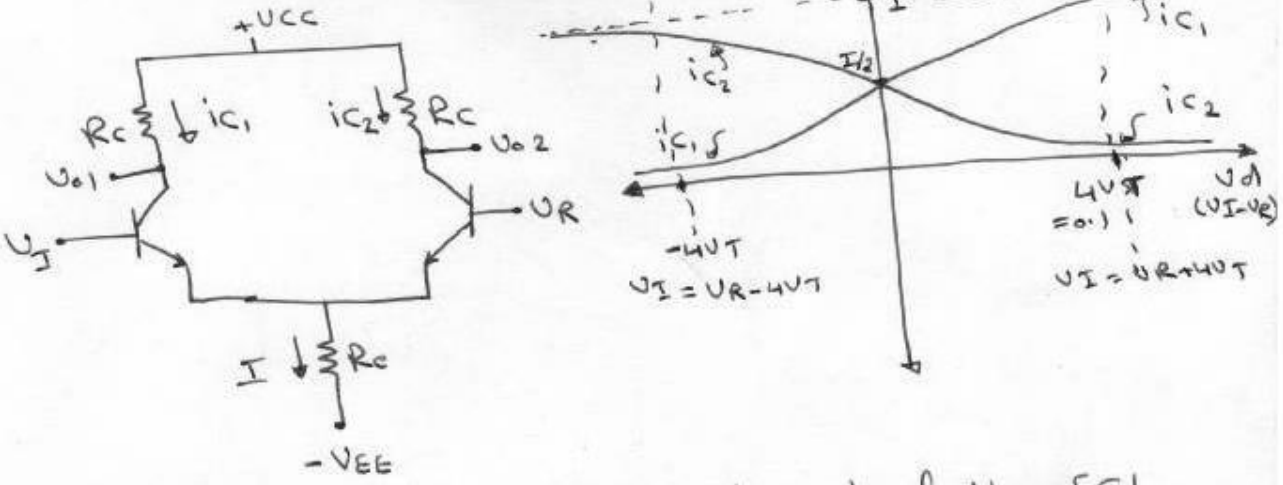
Low power schottky TTL (74LS)



A low-power schottky TTL (LSTTL) gate

Emitter-coupled Logic (ECL)

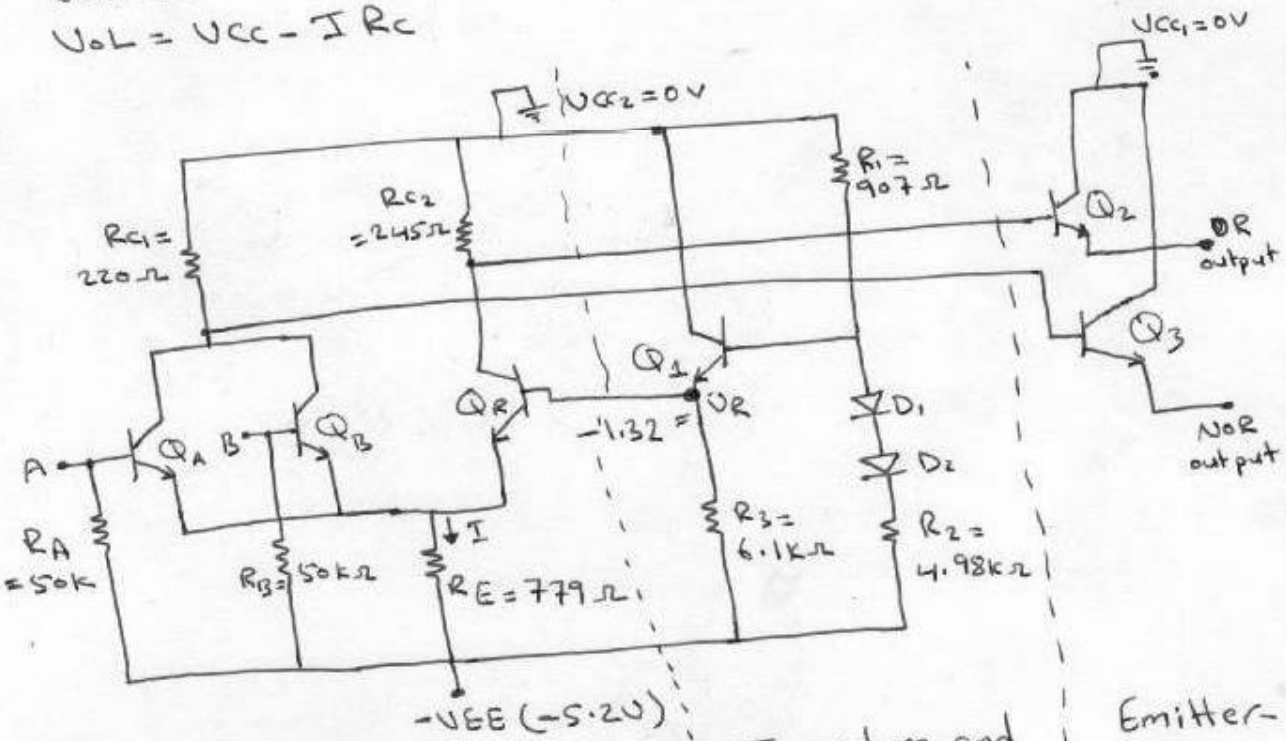
ECL is the fastest logic circuit family.



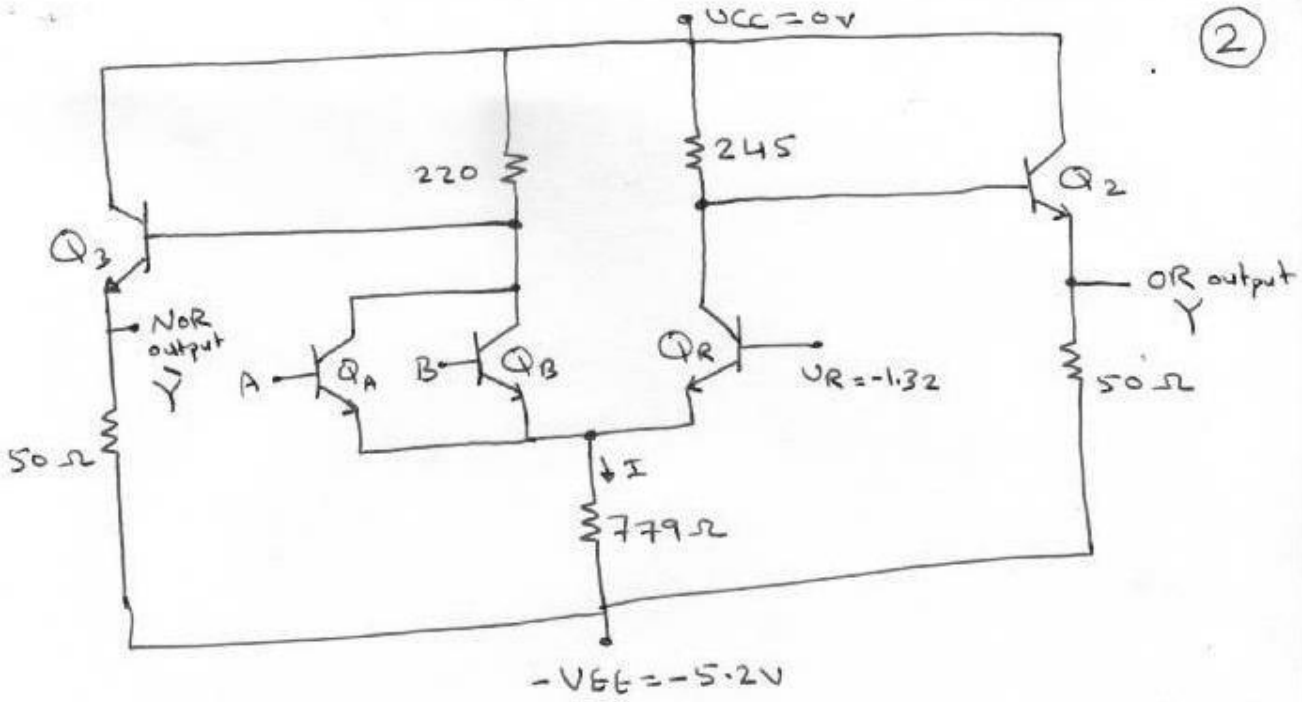
differential amplifier (Basic element of the ECL family).

$V_{OH} = V_{CC}$

$V_{OL} = V_{CC} - I R_C$



ECL basic gate (OR and NOR



Simplified ECL in order to calculate the output voltage levels

At output Y (OR output) :-

(a) If all inputs (A and B in this case) are low then assume Q_A and Q_B are off and Q_R is conducting.

$$V_E = -1.32 - 0.7$$
$$= -2.02\ V$$

$$I = \frac{-2.02 + 5.2}{779} = 4.08\ mA.$$

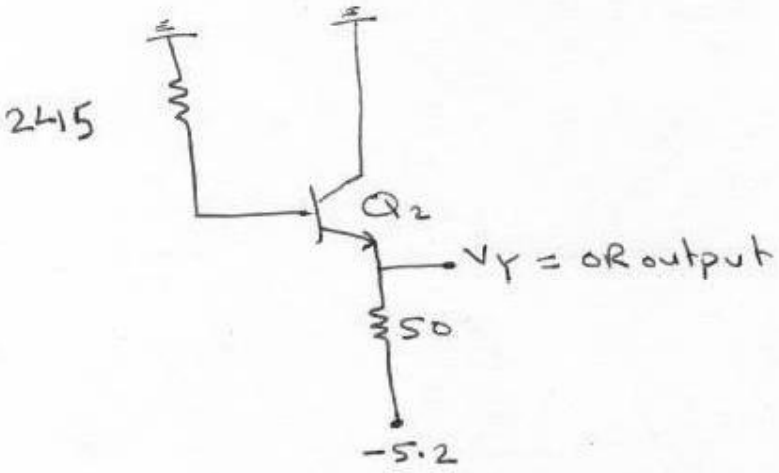
$$V_Y = -0.245 * I - V_{BE_2}$$
$$= -0.245 * 4.08 - 0.7$$
$$= -1.7\ V = V(0)$$

If A and B are at $V(0) = -1.7\,V$ and $V_E = -2.02\,V$

then V_{BE_A} and $V_{BE_B} = -1.7 + 2.02 = 0.32$

then Q_A and Q_B are not conducting

*If at least one of the inputs is high then its corresponding transistor (Q_A or Q_B) is conducting and Q_R is off.



assume $\beta_2 = 100$

$$I_B * 245 + 0.7 + 50 * I_E = 5.2$$

$$I_B * 245 + 0.7 + 50 * I_B(1+100) = 5.2$$

$$I_B = 0.85\ mA.$$

$$V_Y = -0.908 = V(1) = V_H$$

when all inputs (inputs A and B in this case) are high at $V(1) = -0.908$

then $V_E = -0.908 - 0.7 = -1.608\ V$

$$I = \frac{-1.608 + 5.2}{0.779k} = 4.6mA .$$

The emitter followers shift the level of the output signals by one V_{BE} drop. These shifted levels are needed in order that one gate can drive another. This compatibility of logic levels at input and output is an essential requirement in the design of gate circuits.

ECL advantages

1- High speed, the highest of all logic families since transistors do not saturate.

2- Complementary outputs are available which simplifies the logic design.

3- The differential nature of the circuit makes it less effected by noise.

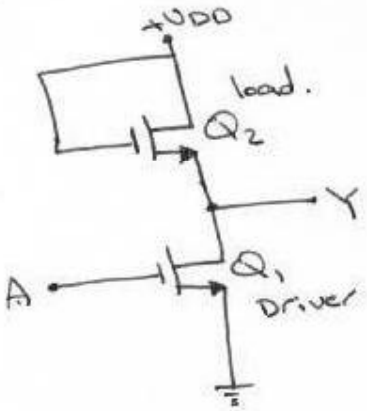
ECL disadvantages:-

① The power dissipation is high as compared to other logic families.

MOSFET

* MOSFET circuits are slower than corresponding BJT circuits because of the parasitic capacitance.
* The lower power dissipation and higher packing density of MOS devices make them more attractive and economical.

MOSFET Inverter:-

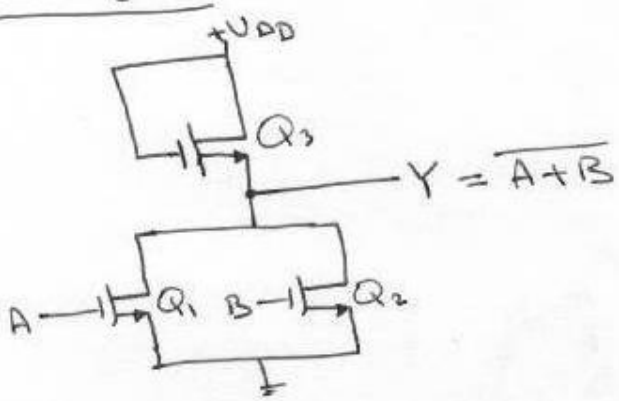


A	Y
VDD	0
0	VDD

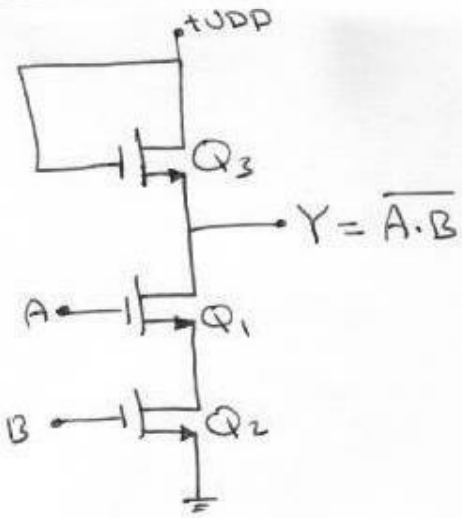
$Y = \bar{A}$

MOSFET Logic gates:-

NOR gate:-



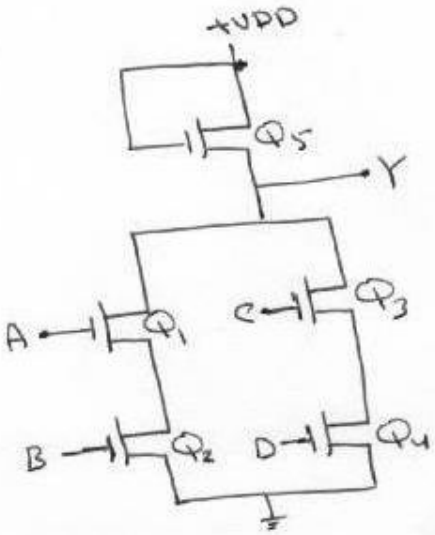
NAND gate:-



Example:-

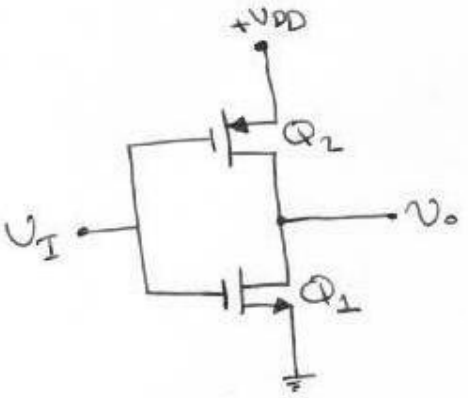
Implement the following function using NMOS logic.

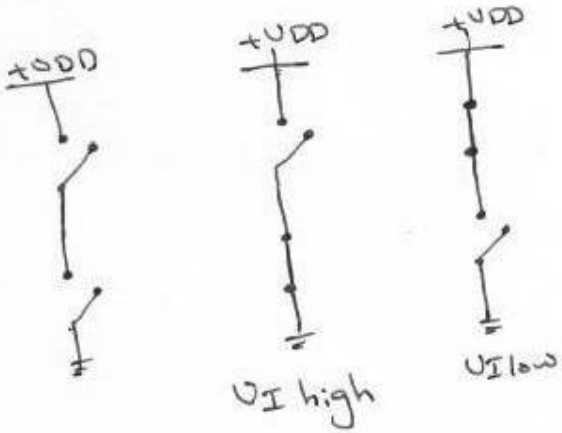
$Y = \overline{AB + CD}$



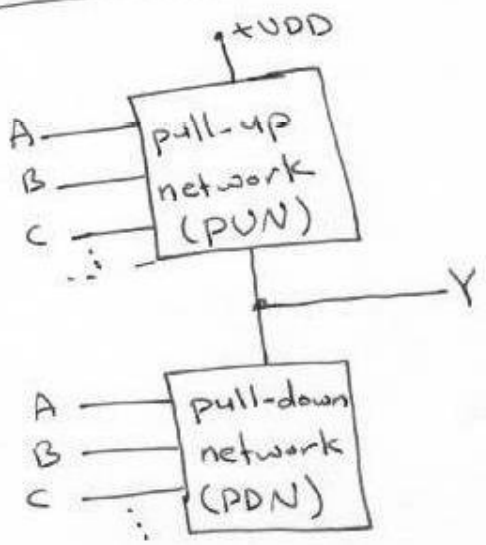
CMOS technology (complementary metal oxide semiconductor)

CMOS Inverter:-



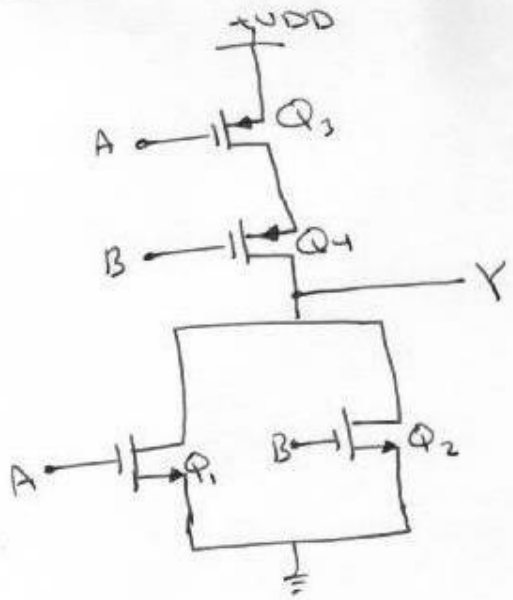


Basic structure of CMOS Logic Circuits:-



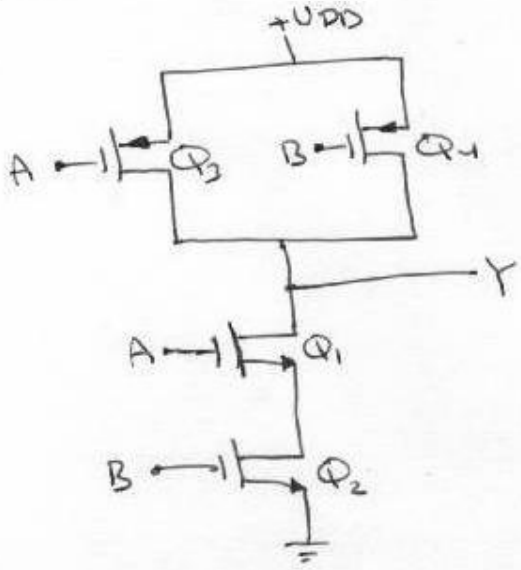
* PDN is constructed from only NMOS transistors, thus PDN is activated when the inputs are high.
* PUN is constructed from only PMOS transistors, thus PUN is activated when the inputs are low.

CMOS NOR gate:-



$$Y = \overline{A+B} = \bar{A}\,\bar{B}$$

CMOS NAND gate:-



$$Y = \overline{AB} = \bar{A}+\bar{B}$$

Example:-

Realize the following logic function using CMOS logic.

$$Y = \overline{A(B+CD)}$$

Sol.:-

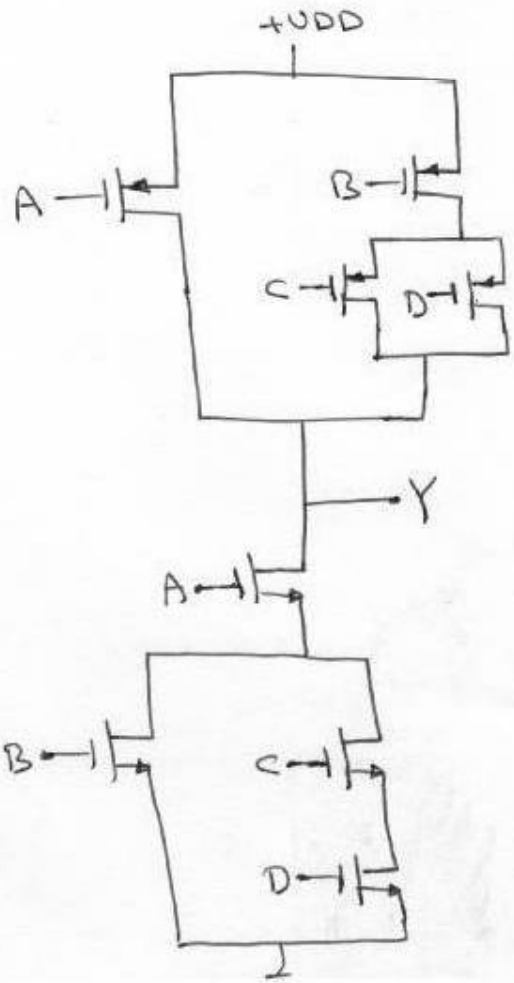
$\bar{Y} = A(B+CD)$ from which PDN is obtained

To obtain the PUN

$$Y = \overline{A(B+CD)}$$

$$Y = \bar{A} + \overline{(B+CD)} = \bar{A} + \bar{B}.\overline{CD}$$

$$Y = \bar{A} + \bar{B}.(\bar{C}+\bar{D}).$$



Example:-

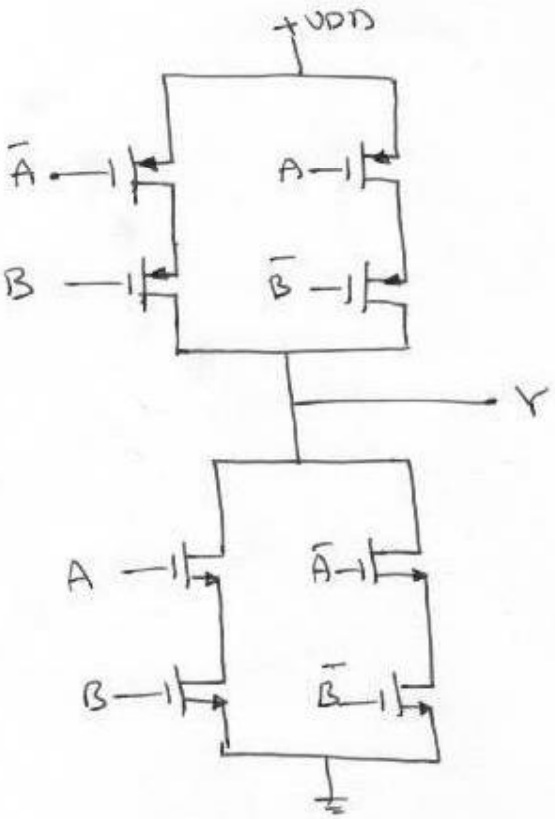
Realize the Exclusive-OR Function:-

$Y = A\bar{B} + \bar{A}B$ using CMOS logic.

Sol.:-

$Y = A\bar{B} + \bar{A}B$ from which PUN is obtained

$\bar{Y} = AB + \bar{A}\bar{B}$



Using direct method

H.w/ Solve the same example using the duality property.

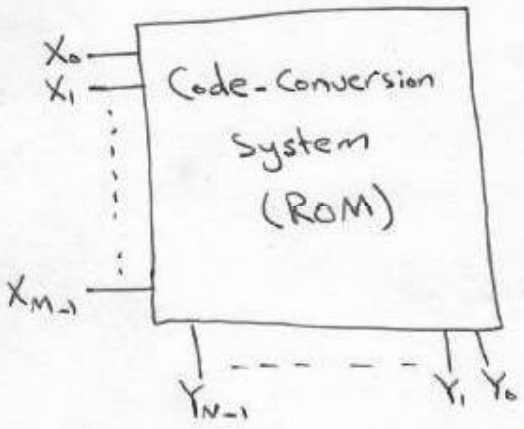
Semiconductor Memories:-

1- Read only Memory : (ROM)

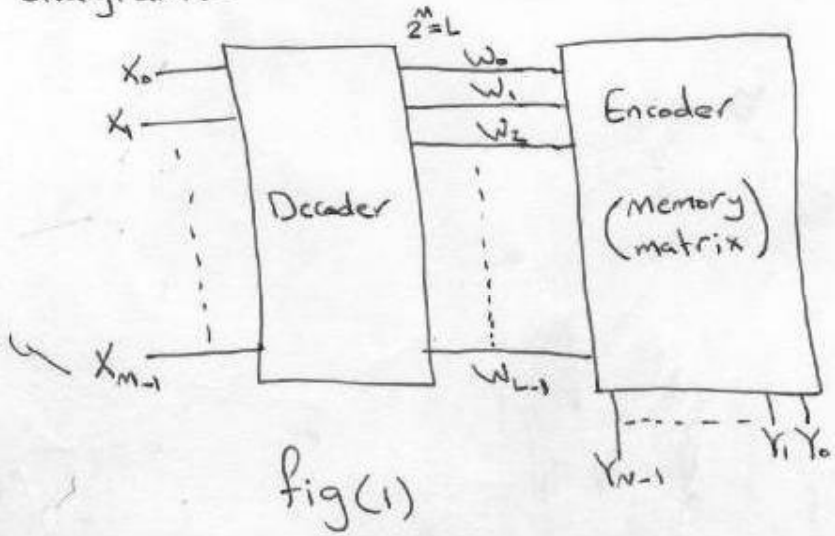
ROM is a memory that can be viewed as a combinational Logic circuit that contains fixed data patterns.

A ROM is a nonvolatile memory, meaning that the data is not lost with power supply switch off.

A ROM can be considered as a code-conversion system as in the following block diagram:-



which can be achieved as in the following block diagram:-



fig(1)

Consider a 64-bit ROM arranged in 16 words of 4-bit each.

X_3	X_2	X_1	X_0	word line	Y_3 Y_2 Y_1 Y_0 (o/p as required)
0	0	0	0	W_0	
0	0	0	1	W_1	
0	0	1	0	W_2	
0	0	1	1	W_3	
				⋮	as required
1	1	1	1	W_{15}	

Two-Dimensional addressing of a ROM

For a ROM with a large size, the previous decoding arrangment in fig(1) is impractical. The number of gates in the decoder becomes very large. Therefore 2-D addressing (X,Y) addressing is used.

Example:-

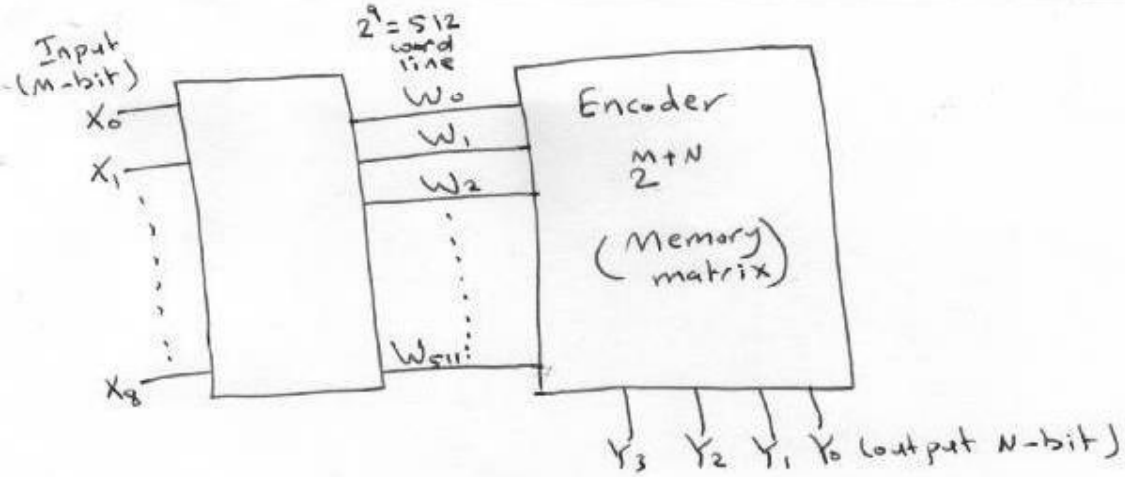
2048-bit (2Kb) with 4-output lines ROM

Sol:-

if the block arrangement of fig(1) is used then

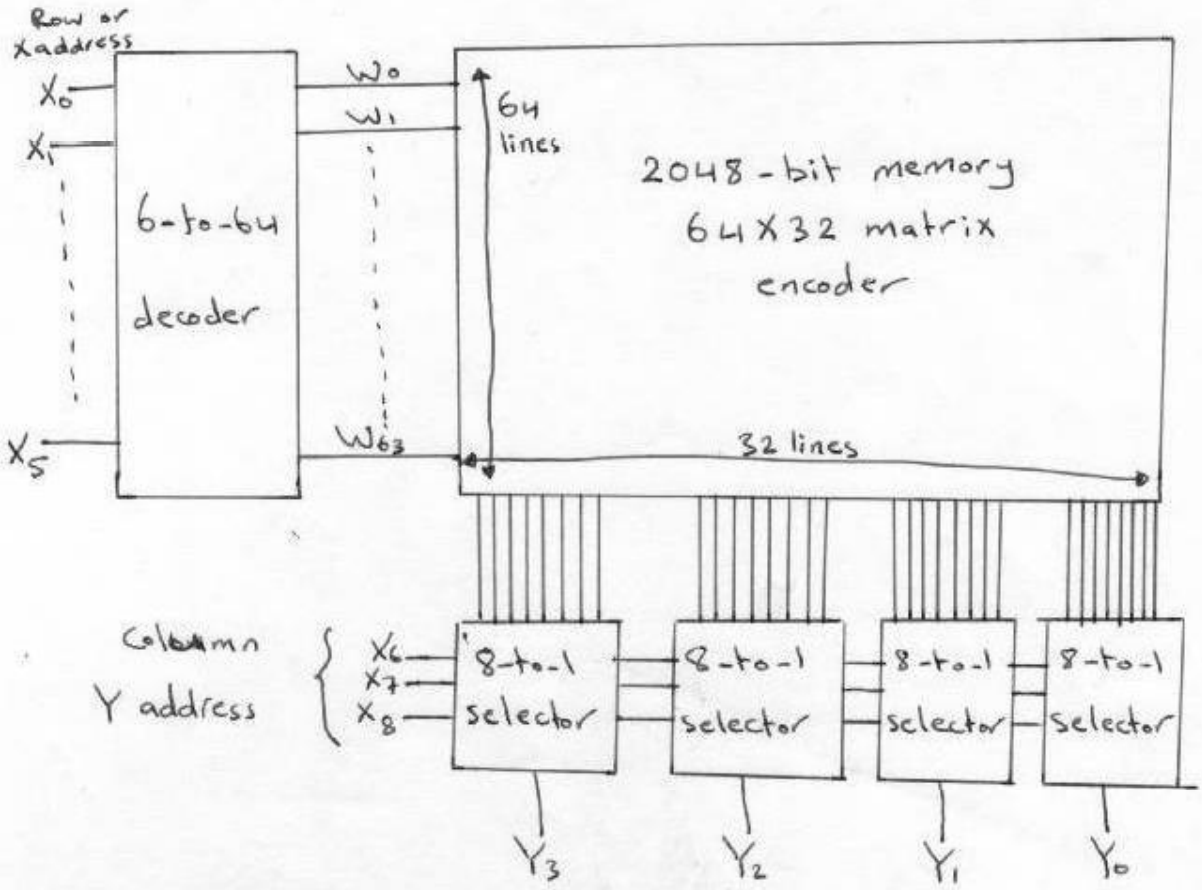
$2048 = 2^{11} = 2^9 * 2^2$

$M = 9, \quad N = 4$



The decoder circuit will require 512 gates (1 for one each word line) which is impractical.

Therefore this 2-Dimensional addressing arrangment is used:-



A 6-bit row address or X address is used which results in 64 word lines (horizontal lines). (4)

If 32 vertical lines are used in the memory matrix which results in $64 \times 32 = 2048$ bits.

However, only four output lines are specified then four 8-to-1 line selectors are used. A 3-bit column address feeds each multiplexer.

Row address Decoder

As an example let us take $M = 3$ with the three address bits denoted X_0, X_1, and X_2 and the 8-word lines denoted $W_0, W_1, \ldots W_7$.

From the truth table we can construct the Row address decoder in an array form using NMOS gates as in the following:-

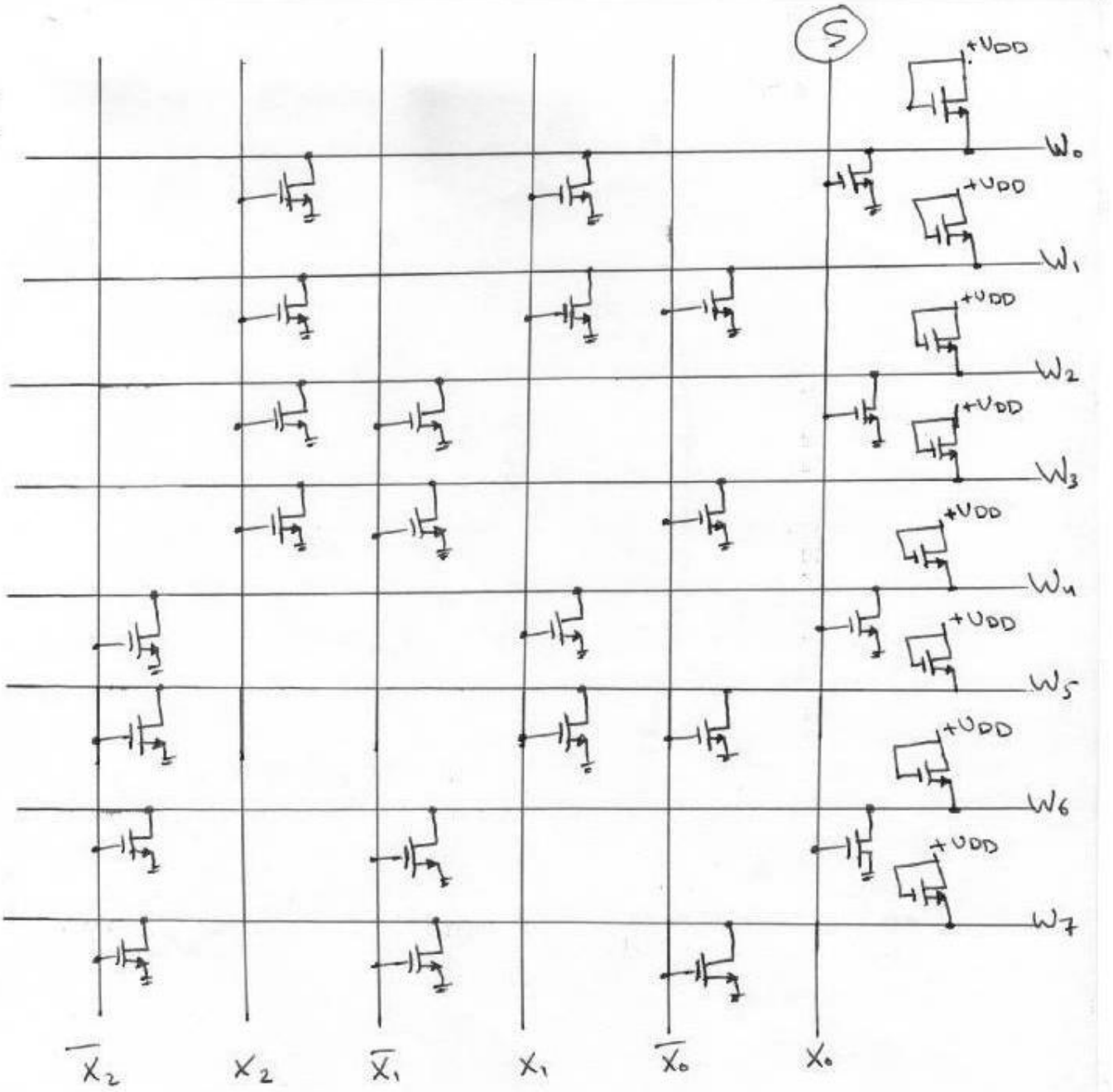
X_2	X_1	X_0	word line
0	0	0	W_0
0	0	1	W_1
0	1	0	W_2
0	1	1	W_3
1	0	0	W_4
1	0	1	W_5
1	1	0	W_6
1	1	1	W_7

$$W_0 = \overline{\overline{X_0}\,\overline{X_1}\,\overline{X_2}}$$

$$W_0 = \overline{X_0 + X_1 + X_2}$$

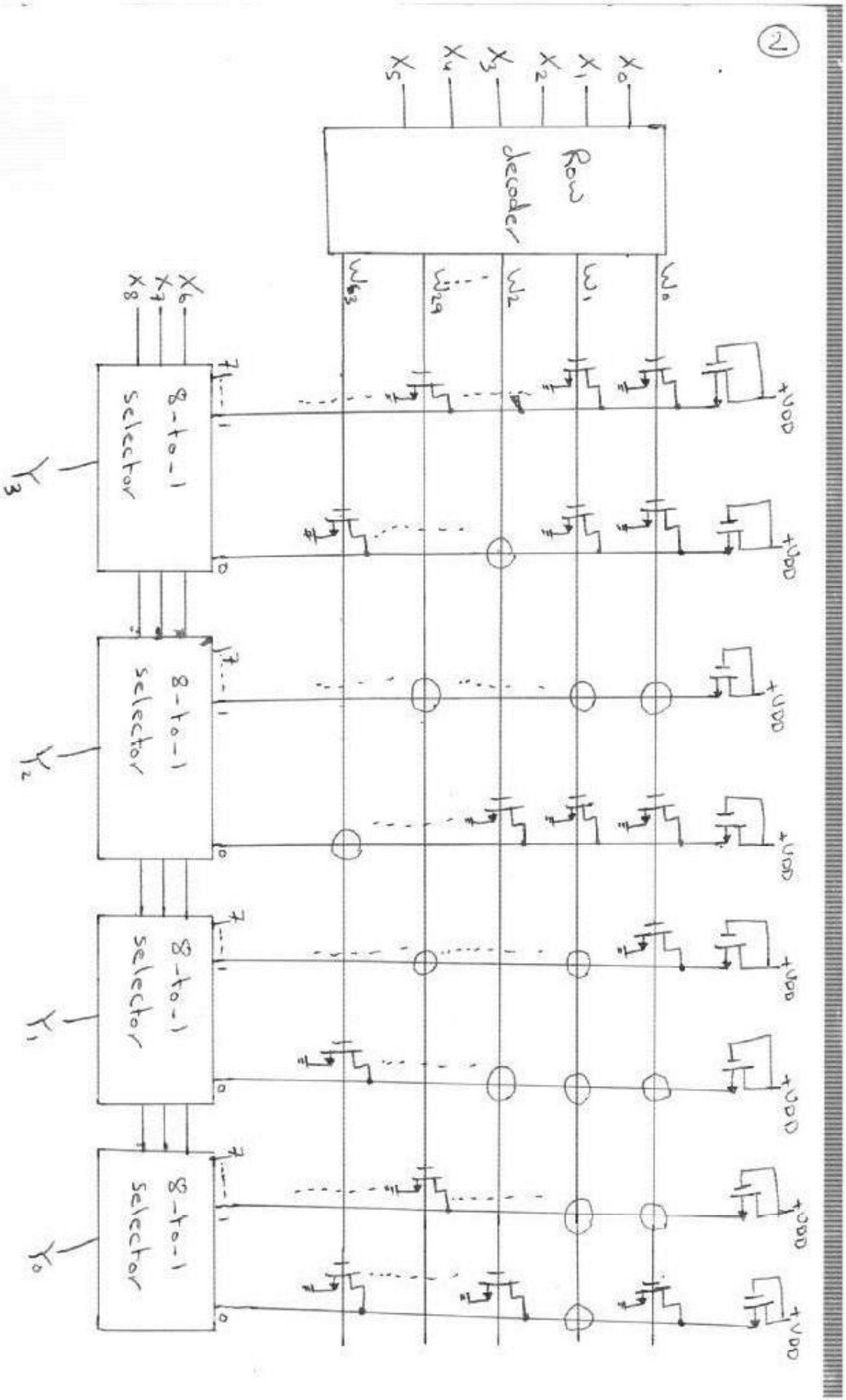
$$W_5 = \overline{\overline{X_0}\,X_1\,X_2}$$

$$W_5 = \overline{\overline{X_0} + X_1 + \overline{X_2}}$$



Memory matrix (encoder)

X_8	X_7	X_6	X_5	X_4	X_3	X_2	X_1	X_0	word line	Y_3	Y_2	Y_1	Y_0
0	0	0	0	0	0	0	0	0	W_0	0	0	1	0
0	0	0	0	0	0	0	0	1	W_1	0	0	1	1
0	0	0	0	0	0	0	1	0	W_2	1	0	1	0
0	0	0	1	1	1	1	1	1	W_{63}	0	1	0	0
0	0	1	0	0	0	0	0	0	W_0	0	1	0	1
0	0	1	0	0	0	0	0	1	W_1	0	1	1	1
0	0	1	0	1	1	1	0	1	W_{29}	0	1	1	0



Random Access Memory :- (RAM)

In a semiconductor memory an array of storage cells is used in constructing a RAM.

Eeach cell is holding 1 bit of data.
A RAM is a voltatile memory, which means that all stored information is lost when power supply is turned off.

Two-Dimensional addressing of a RAM :-

A great economy of the number of gates in the decoder circuit is obtained by arranging the memory cells in a two-dimensional array.

For example :- A 4k bit RAM is organized in a 64X64 array as in the following :-

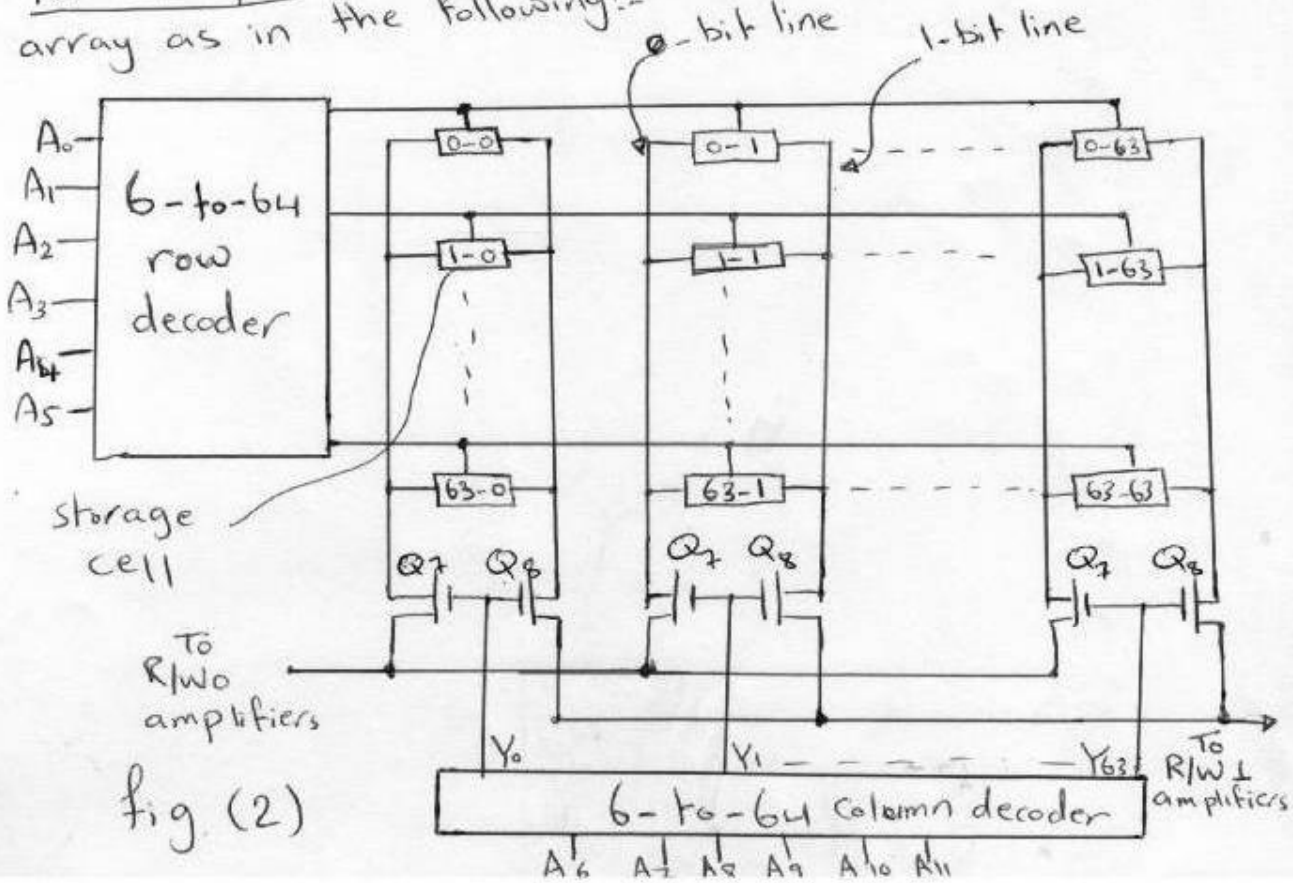
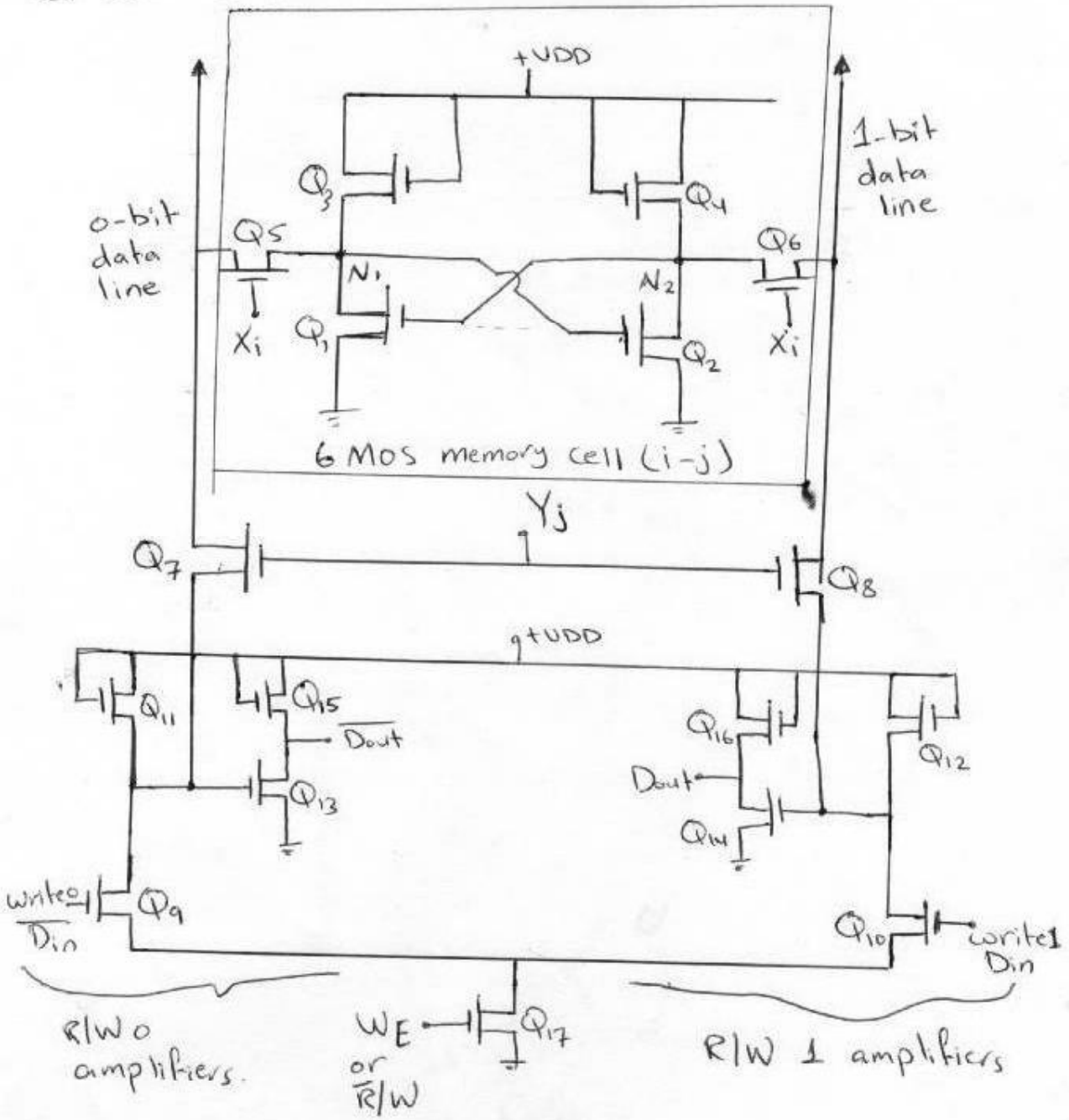


fig (2)

Figure (2) shows the organization of a 4096-word-by-1 bit RAM. (4)

RAM Cells :-

(a) Static MOS RAM



* To select a cell its x and y address should be excited (2-Dimensional) addressing.

* Q_{17} and Q_{10} form an AND gate with inputs W_E and Din. also Q_{17} and Q_9 form an AND gate with inputs W_E and $\overline{Din}$.

where W_E or $\overline{R}/W$ = write enable

Din = Data input

Dout = Data output.

Case I

(write a 1 in the cell)

① address the cell ($X_i = 1$ and $y_j = 1$) so that Q_7, Q_8, Q_5 and Q_6 are conducting.

② set $W_E = 1$, $Din = 1$ and $\overline{Din} = 0$

* then Q_{17} and Q_{10} are ON and Q_9 is off. Hence the 1-bit data line is grounded and 0-bit data line goes to V_{DD} through load Q_{11}.

* Thus node N_2 is effectively grounded.

* So Q_1 is cut off and N_1 rises to V_{DD}.

* N_1 is tied to the gate of Q_2 therefore Q_2 is held ON and N_2 is maintained at 0V.

* when the address is removed (Q_5, Q_6, Q_7 and Q_8 are off), Q_2 is ON, Q_1 is off, and a 1 has been written into the selected memory cell.

Case II (read a 1 stored in a memory cell)

① Set $X_i = 1$ and $Y_j = 1$

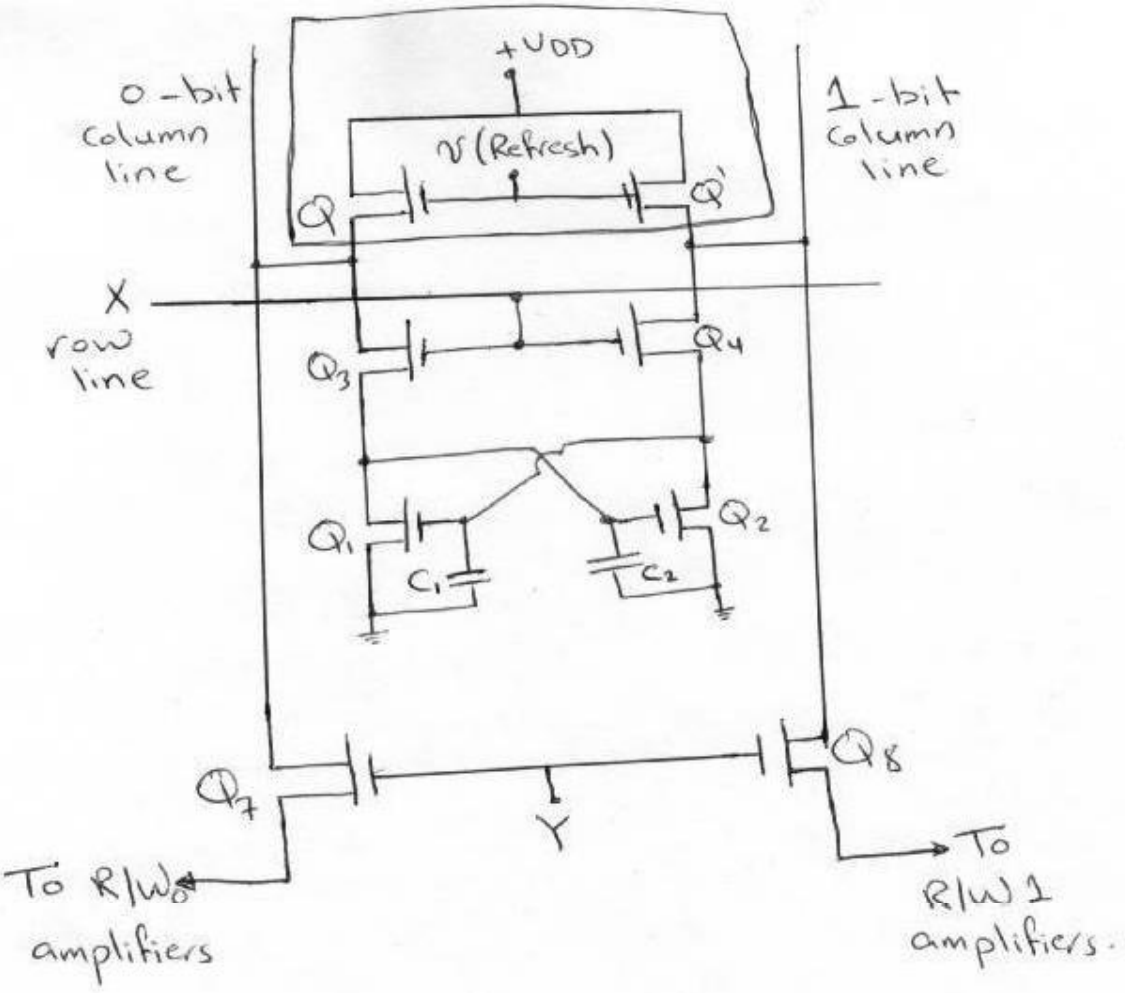
② assume that a 1 is stored in this cell so Q_2 is ON and Q_1 is off (N_2 is at 0V and N_1 is at V_{DD}).

③ Set $W_E = 0$.

* Then Q_{17} is off and hence Q_{10} and Q_9 are non conducting.
* So the 1-bit data line and the 0-bit data line are connected to V_{DD} through load Q_{12} and Q_{11} respectively.
* since Q_2 is ON (N_2 at 0V) then the 1-bit line is effectively grounded.
* therefore Q_{14} is off and Dout $= V_{DD}$ (logic 1).
* Since Q_1 is off then 0-bit data line is at V_{DD}.
* therefore Q_{13} is ON and $\overline{\text{Dout}} = 0$

So we have read 1 stored in cell (i,j).

Dynamic RAM Cell:-



In the Dynamic RAM cell, information is stored as charge on the two capacitors C_1 and C_2.

If a 1 is written in the cell then C_2 is charged to V_{DD} and C_1 is charged to 0 volt, so that Q_2 is ON and Q_1 is off.

In DRAM the capacitors which store the information will discharge slowly because of the leakage currents and information may be lost.

Therefore DRAM require periodic refreshing to regenerate the data stored on capacitors.

The two transistors (Q and Q') are added to refresh each cell in a given column.

If we have a RAM with 64 columns then 64 of such circuitry (Q and Q') is needed to refresh a cell in that column.

ν is a pulse of less than 1 μsec occurring about every 2 msec.

If X_1 is high and ν is also high then row(1) will be refreshed simultaneously.

Because X_1 is high then Q_3 and Q_4 are ON, and because ν (Refresh) is high then Q and Q' are ON.

Assume that Q_1 is off and Q_2 is ON (storing a 1). Then during the refresh interval a current will flow in Q and Q_3 charging C_2 toward V_{DD} and since Q_1 is off all the current from V_{DD} is directed toward C_2.

As for the current in Q' and Q_4 then C_1 will not be charged because Q_2 is conducting. So the cell is restored to its original state.