Registers

Logic circuit has two parts:

- Combinational cct. : o/p depended on current i/p
- Sequential cct. : o/p depended on current i/p and past i/p, it has a memory element which is known as a flip flop

The flip flop is several logic gates connected together in way that permit information to be stored.

One flip flop can be store one bit and it is called a memory cell.

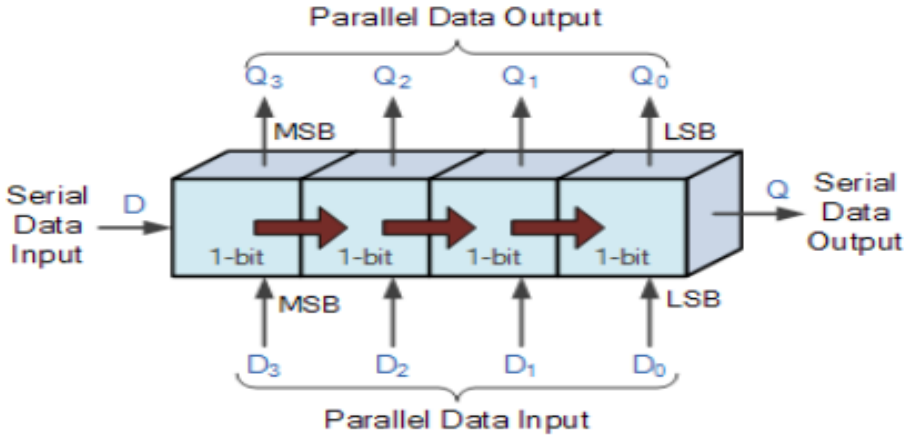
To increase number of bits to be store we have to use a group of flip flops, the group of flip flops is called a register.

The n-bit register consist of n number of flip flops and it is capable of storing an n-bit word.

Ex: 4-bit register used four flip flops and can be store 4 bits.

Register: is a combinational of FF's used to store data

The synchronous sequential circuit loads the data present on its inputs and the moves or shifts it to its output once every clock cycle it is called shift register

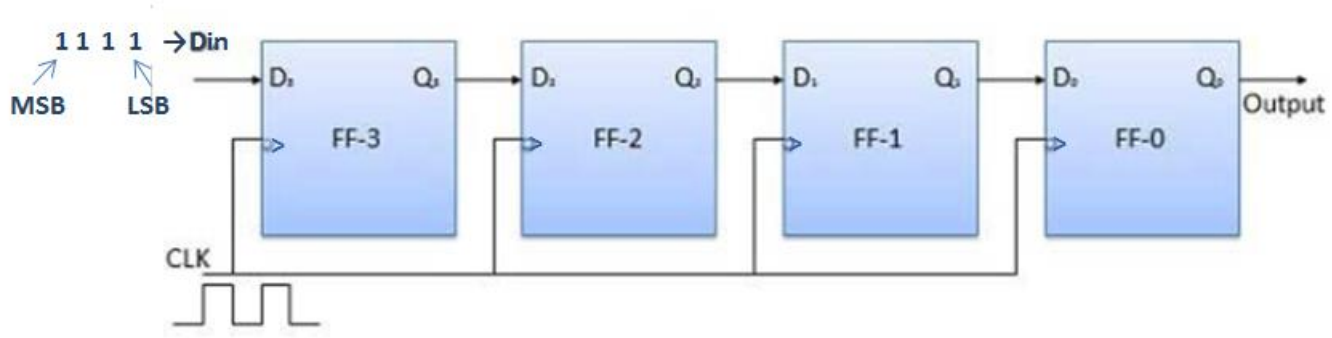


There are four mode of operations of a shift register:

- Serial input serial output **SISO**
- Serial input parallel output **SIPO**
- Parallel input serial output **PISO**
- Parallel input parallel output **PIPO**

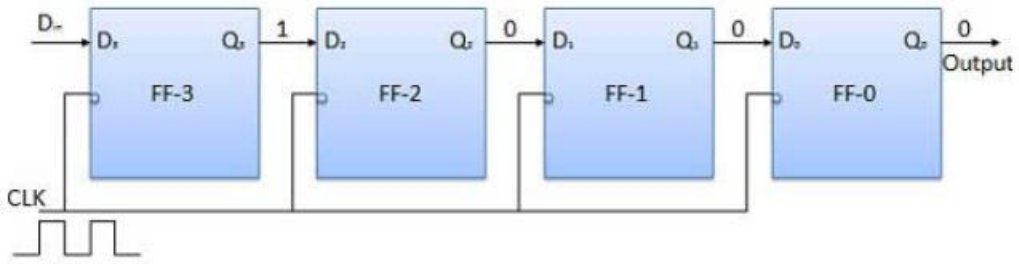
SISO: Serial Input Serial Output

To entry a four bit binary number (1111) into register , this number should be applied to Din bit with the LSB bit applied first

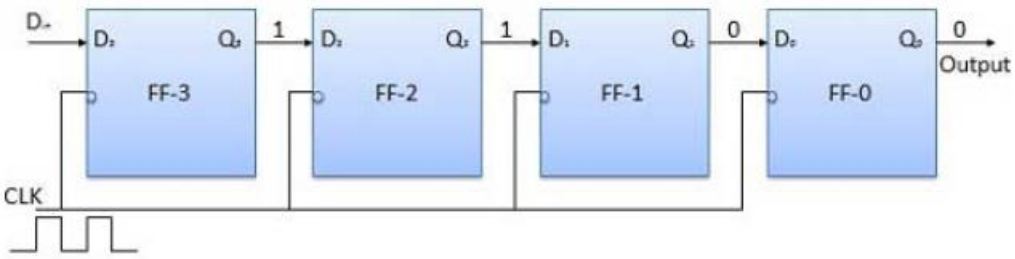


Let all the flip-flop be initially in the reset condition $Q_3 = Q_2 = Q_1 = Q_0 = 0$.

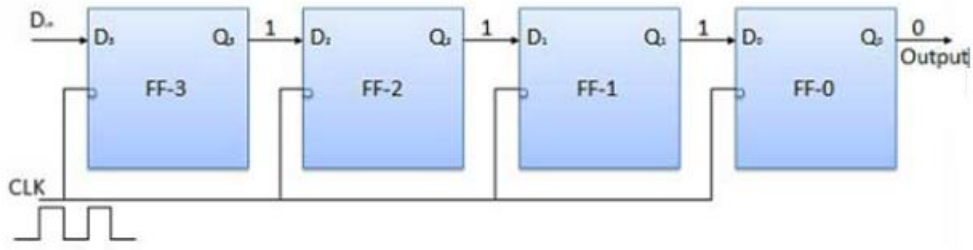
$D_{in} = D_3 = 1$. Apply the clock. The FF-3 is set, and stored word in the register is $Q_3\ Q_2\ Q_1\ Q_0 = 1000$.



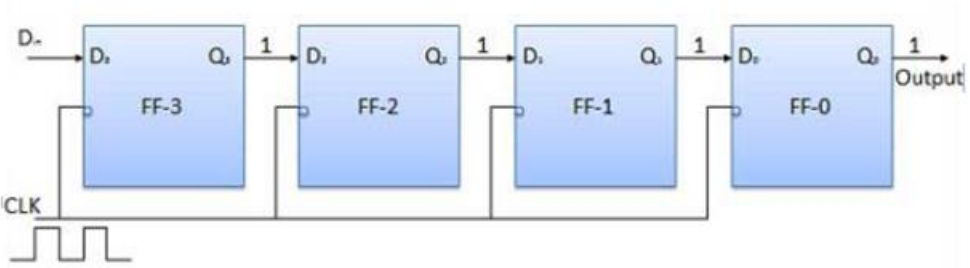
Apply the next bit to D_{in}. So $D_{in} = 1$. As soon as the next negative edge of the clock hits, FF-2 will set and the stored word change to $Q_3\ Q_2\ Q_1\ Q_0 = 1100$.



Apply the next bit to be stored 1 to D_{in}. Apply the clock pulse. As soon as the third negative clock edge hits, FF-1 will be set and output will be modified to Q_3 Q_2 Q_1 Q_0 = 1110.



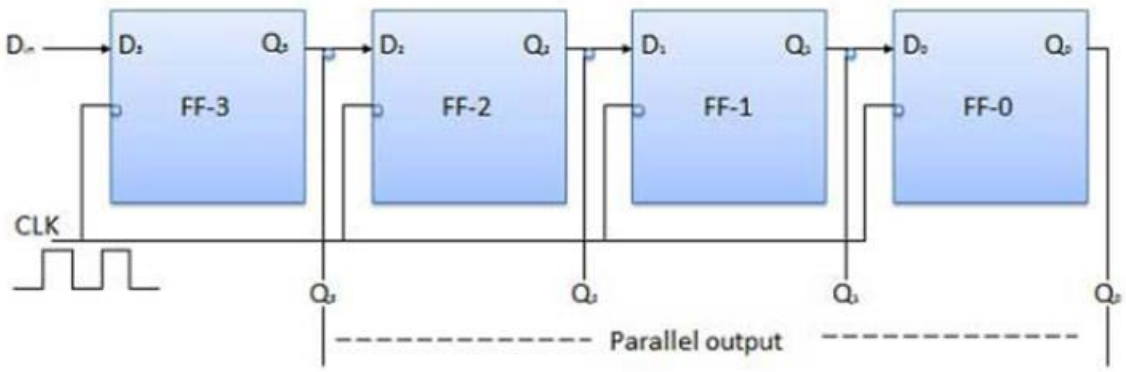
Similarly with D_{in} = 1 and with the fourth negative clock edge arriving, the stored word in the register is Q_3 Q_2 Q_1 Q_0 = 1111.



	CLK	$D_n = Q_3$	$Q_3 = D_2$	$Q_2 = D_1$	$Q_1 = D_0$	Q_0
Initially			0	0	0	0
(i)	↓	1	1	0	0	0
(ii)	↓	1	1	1	0	0
(iii)	↓	1	1	1	1	0
(iv)	↓	1	1	1	1	1

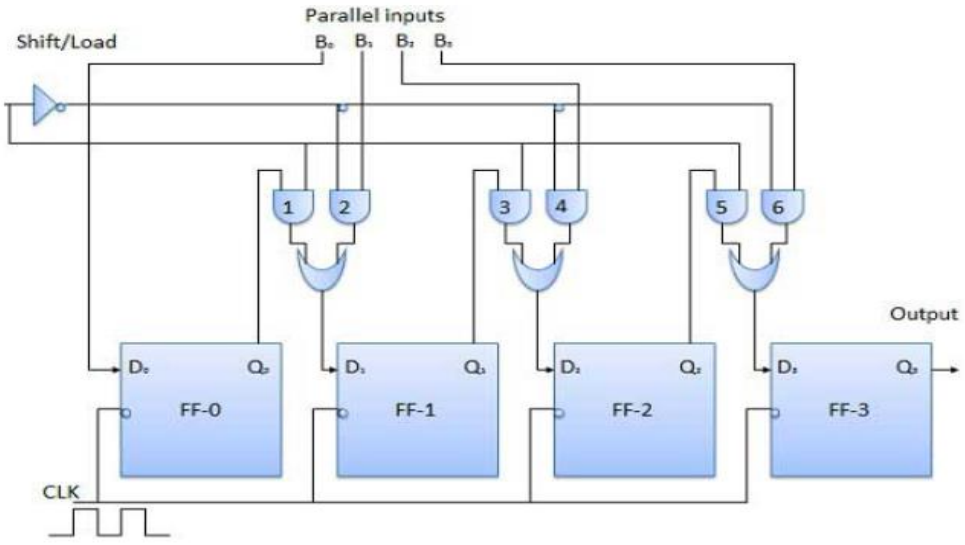
→ Direction of data travel

SIPO: Serial Input Parallel Output



- In such types of operations, the data is entered serially and taken out in parallel fashion.
- Data is loaded bit by bit. The outputs are disabled as long as the data is loading.
- As soon as the data loading gets completed, all the flip-flops contain their required data, the outputs are enabled so that all the loaded data is made available over all the output lines at the same time.
- 4 clock cycles are required to load a four bit word. Hence the speed of operation of SIPO mode is same as that of SISO mode.

PISO: Parallel Input Serial Output



- Data bits are entered in parallel fashion.
- The circuit shown below is a four bit parallel input serial output register.
- Output of previous Flip Flop is connected to the input of the next one via a combinational circuit.
- The binary input word B_0, B_1, B_2, B_3 is applied though the same combinational circuit.
- There are two modes in which this circuit can work namely - shift mode or load mode.

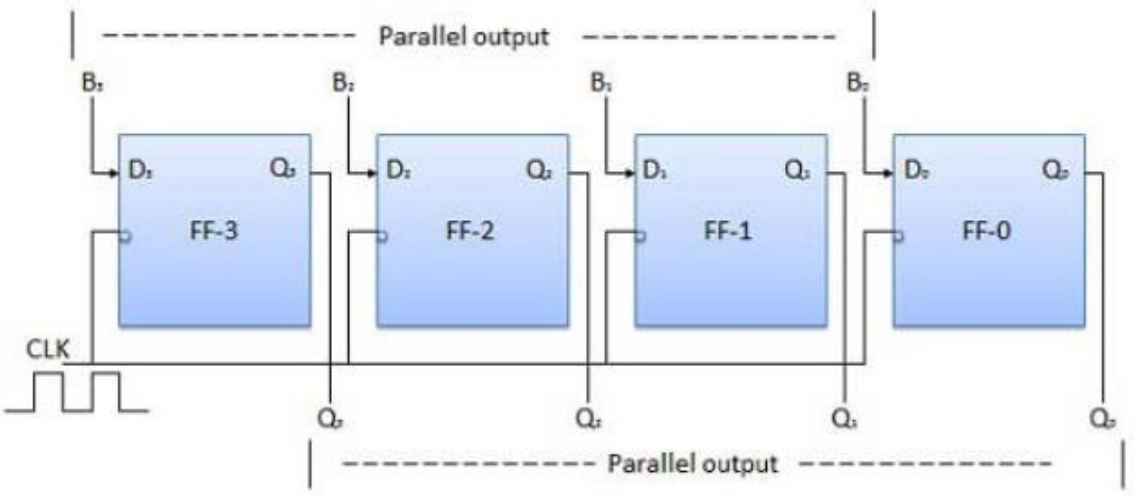
Load mode

When the shift/load bar line is low (0), the AND gate 2, 4 and 6 become active they will pass B_1, B_2, B_3 bits to the corresponding flip-flops. On the low going edge of clock, the binary input B_0, B_1, B_2, B_3 will get loaded into the corresponding flip-flops. Thus parallel loading takes place.

Shift mode

When the shift/load bar line is low (1), the AND gate 2, 4 and 6 become inactive. Hence the parallel loading of the data becomes impossible. But the AND gate 1,3 and 5 become active. Therefore the shifting of data from left to right bit by bit on application of clock pulses. Thus the parallel in serial out operation takes place.

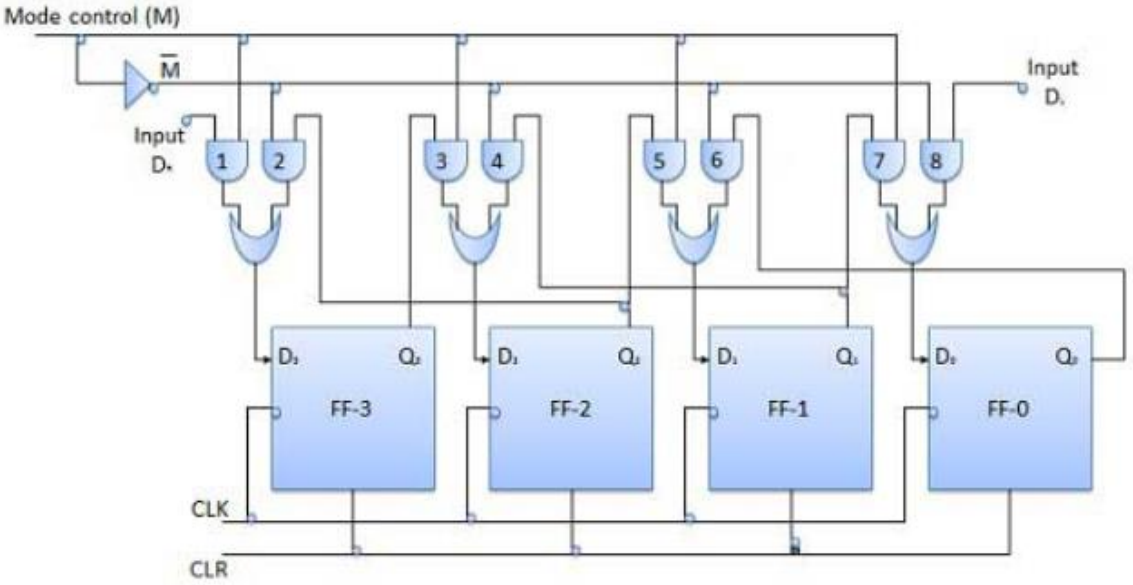
PIPO: Parallel Input Parallel Output



In this mode, the 4 bit binary input B_0, B_1, B_2, B_3 is applied to the data inputs D_0, D_1, D_2, D_3 respectively of the four flip-flops. As soon as a negative clock edge is applied, the input binary bits will be loaded into the flip-flops simultaneously. The loaded bits will appear simultaneously to the output side. Only clock pulse is essential to load all the bits.

Bidirectional Shift Register

- If a binary number is shifted left by one position then it is equivalent to multiplying the original number by 2. Similarly if a binary number is shifted right by one position then it is equivalent to dividing the original number by 2.
- Hence if we want to use the shift register to multiply and divide the given binary number, then we should be able to move the data in either left or right direction.
- Such a register is called bi-directional register. A four bit bi-directional shift register is shown in fig.
- There are two serial inputs namely the serial right shift data input DR, and the serial left shift data input DL along with a mode select input (M).



With M = 1 Shift right operation:

If M = 1, then the AND gates 1, 3, 5 and 7 are enabled whereas the remaining AND gates 2, 4, 6 and 8 will be disabled.

The data at D_R is shifted to right bit by bit from FF-3 to FF-0 on the application of clock pulses. Thus with M = 1 we get the serial right shift operation.

With M = 0 Shift left operation:

When the mode control M is connected to 0 then the AND gates 2, 4, 6 and 8 are enabled while 1, 3, 5 and 7 are disabled.

The data at D_L is shifted left bit by bit from FF-0 to FF-3 on the application of clock pulses. Thus with M = 0 we get the serial right shift operation.