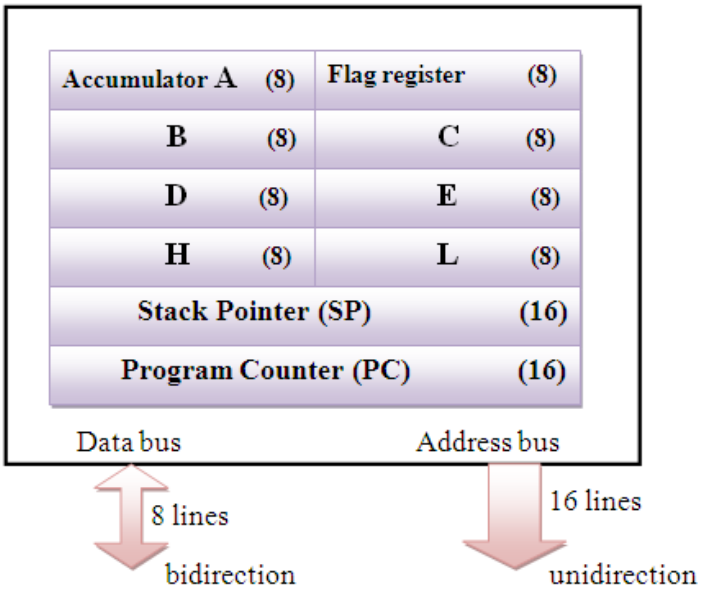
Overview of 8085 microprocessor

The main features of 8085 mp are:

- It is a 8 bit microprocessor.
- It has 16-bit address bus and hence can address up to 2^{16} = 65536 bytes (64KB) memory locations through A0-A15 .
- The first 8 lines of address bus and 8 lines of data bus are multiplexed AD0 – AD7 .
- Data bus is a group of 8 lines D0 – D7 .
- It supports external interrupt request.
- A 16 bit program counter (PC) register
- A 16 bit stack pointer (SP) register
- Six (8-bit) general purpose register arranged in pairs: BC, DE, HL and accumulator (8-bit) register and flag register.
- It requires a signal +5V power supply and operates at 3.2 MHZ single phase clock.
- It is enclosed with 40 pins .

The 8085 programmable registers: -



Registers: -

The 8085 mp has six general –purpose 8 bit register to store data during program execution. These registers are identified as B, C, D, E, H and L, they can be combined as register pair BC, DE and HL to perform some 16- bit operations.
These registers are programmable, meaning that a programmer can use them to load or transfer data from the registers by using instructions.
EX: -

MOV B,C : transfer the data from register C
to register B

Accumulator: -

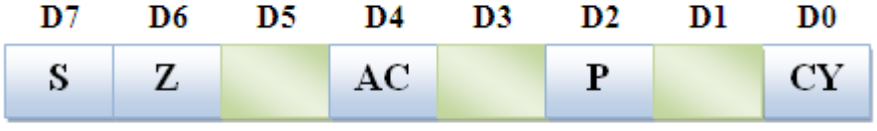
The accumulator is an 8-bit register that is part of the arithmetic logic unit (ALU).
This register is used to store 8 bit data and to perform arithmetic and logical operations
The result of an operation is stored in the accumulator.
The accumulator also identified as register A.

Flags: -

The ALU includes five flip- flops that are set or reset according to data conditions in the accumulator and other registers.

The 8085 has flag register to indicate five different types of data conditions
Zero (Z), carry (CY), sign (S), parity (P) and auxiliary carry (AC)

The bit positions for these flags in the flag register are as follows: -



- **S- Sing flag: -**

After the execution of an arithmetic or logic operation, if bit D7 of the result (usually in the accumulator) is 1. The sign flag is set.
This flag is used with signed number.
In a given byte, if

D7=1 ⟶ the number will be viewed as negative
D7=0 ⟶ the number will be considered positive

- **Z- Zero flag: -**

The zero flag is set if the ALU operation result in zero, and the flag is reset if the result is not zero.
This flag is modified by the results in the accumulator as well as in the other registers.

- **AC- Auxiliary Carry flag: -**

In an arithmetic operation, when a carry is generated by digit D3 and passed on to digit D4, the AC flag is set.
This flag is used only for BCD (Binary Coded Decimal) operations.

- **P- Parity flag: -**

After an arithmetic or logic operation if the result has an even number of 1's the flag is set. If it has an odd number of 1's, the flag is reset.

EX: - the data byte 0000 0011 has even number of 1's, so it has even parity even if the magnitude of number is odd.

- **CY- Carry flag: -**

If an arithmetic operation results in a carry, the carry flag is set, otherwise it is reset, the carry flag also serves as a borrow flag for subtraction.

EX1: - Add the number 35 H to the number 4A H

4A	0100 1010
35	0011 0101
	0111 1111 = 7F H

Flag status:

S=0. Z=0, AC=0, P=0, CY=0

EX2: - Add the number FF H to the number 01 H

FF	1111 1111
01	0000 0001
1	0000 0000 = 00 H, CY=1

Flag status:

S=0. Z=1, AC=1, P=1, CY=1

Program Counter (PC): -

16-bit register, the program counter is used to sequence the execution of a program.
The function of the program counter is to point to the memory address from which the next byte is to be fetched. When a byte (machine code) is being fetch the PC is increment by one to point to the next memory location.

Stack Pointer (SP): -

16-bit register, the stack pointer is used as a memory pointer for the stack memory.

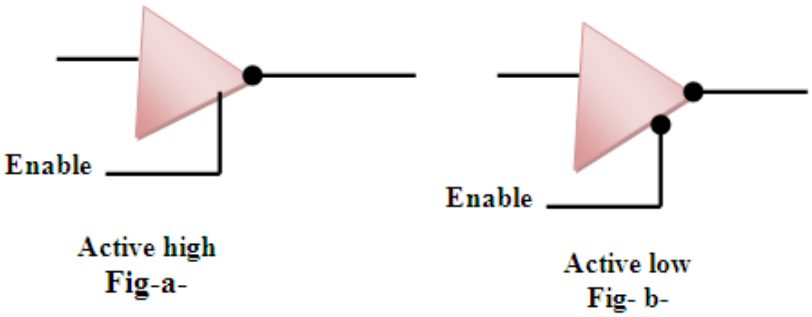
Stack: - is a group of memory location in RAM memory, the stack is used to store binary information temporarily during the execution of a program.

- **Tri-state devices:-**

tri-state logic device have three states

1- Logic 1
2- Logic 0
3- High impedance

A tri-state logic device has a third line called enable as shown

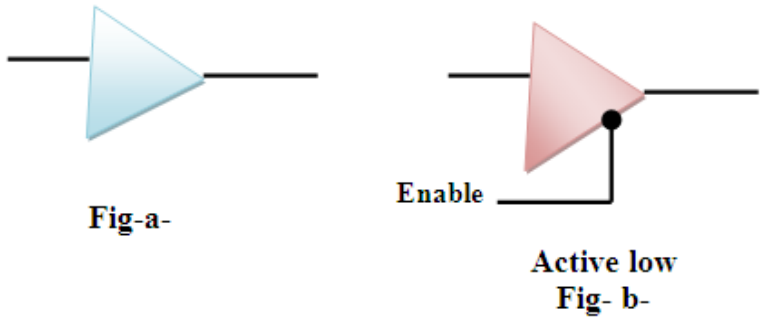


Tri-State Inverters

Fig-a- shows a tri-state inverter with active high, when the enable is high the circuit function as an ordinary inverter, and when the enable line is low, the inverter stays in the high impedance state.

- **Buffer: -**

The buffer is a logic circuit, which amplifies the current or power; it has one input line and one output line



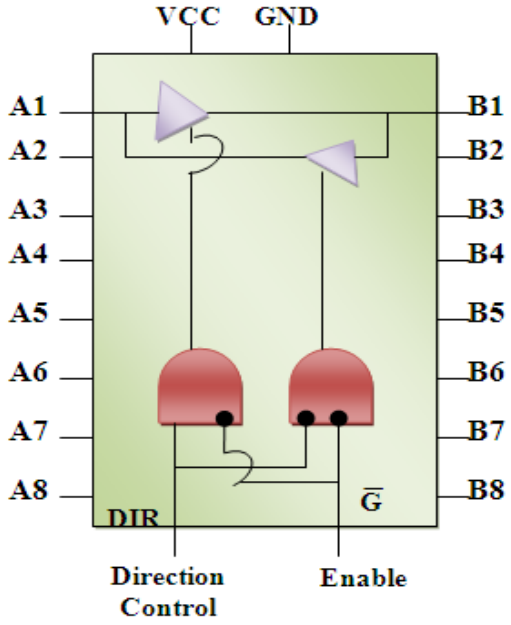
Simple buffer is shown in fig-a-, the logic level of the output is the same as that of the input

1 ⟶ input provides output ⟶ 1 (opposite of an inverter)

Fig-b- shows a tri-state buffer, when enable line is low, the circuit functions as a buffer otherwise it stays in high impedance state.
The buffer is commonly used with the data bus and address bus.

- **Bidirectional buffer: -**

The data bus of a microcomputer system is bi-directional. Therefore, it requires a buffer that allows data to flow in both directions.
Fig-a- shows the logic diagram of the bidirection buffer 74LS245

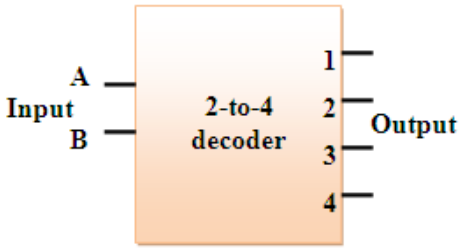


Enable $\overline{G}$	Direction Control DIR	operation
L	L	Data flow From B to A
L	H	Data flow From A to B
H	X	High impedance

The 74LS245 includes sixteen-bus driver, eight for each direction, with tri-state output, the direction of data flow is control by the pin DIR, the enable signal $\overline{G}$ (active low) and DIR signal are ANDed to active the bus lines.

- **Decoder: -**

The decoder is a logic circuit that identifies each combination of the signals present at its input
EX: if the decoder has two input lines the decoder will have four output lines as shown



I/P		O/P			
B	A	0	1	2	3
0	0	1	0	0	0
0	1	0	1	0	0
1	0	0	0	1	0
1	1	0	0	0	1

Fig-a-

If the input is 11, the output line 3 will be at logic 1, and the others will remain at logic 0 this is called decoding.

Fig-a- shows 2:4 decoder, it is also called a 1-out-of-4 decoder

Various types of decoders are available like 3-to-8, 4 to 16, some decoder have active low output lines as well as enable lines

Fig-b- shows decoder will not function unless it is enabled by a low signal

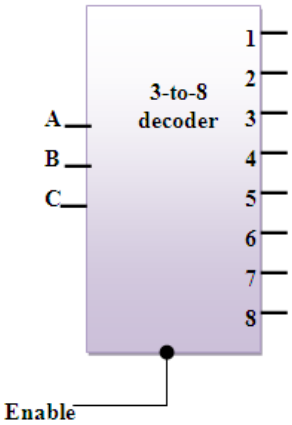


Fig-b-
Decoder with enable

A decoder is commonly used device in interfacing I/O peripheral and memory

Decoders are built also internal to a memory chip to identify individual memory locations.

- **latch: -**

a latch is a D flip-flop, two type of D flip-flops are available: -

1- Transparent latch
2- Positive- edge- triggered flip-flop

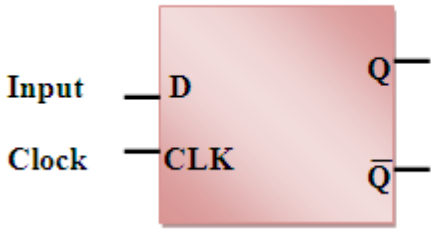


Fig-a-

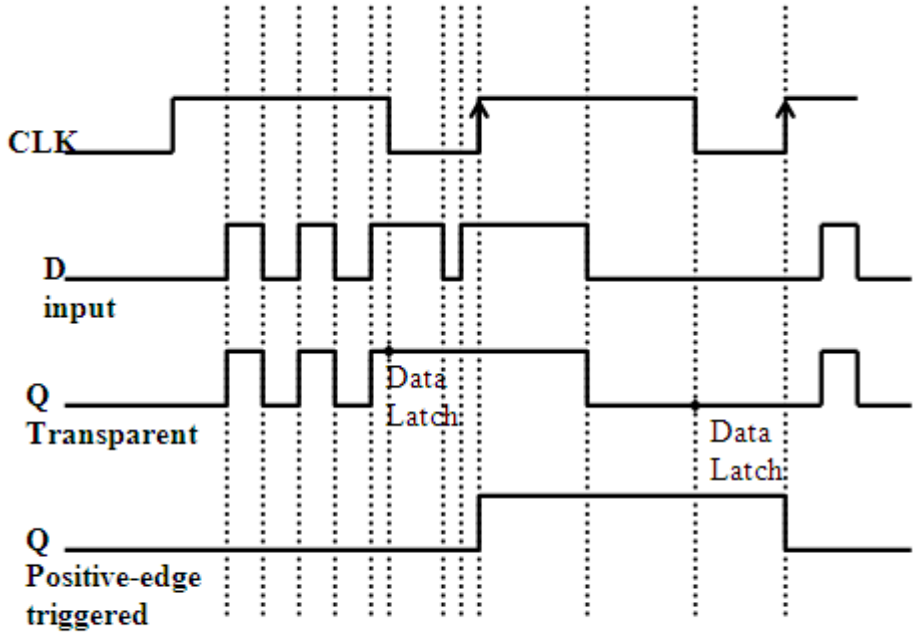


Fig-b-

In transparent latch, when the clock signal is high, the output Q changes according to the input D. when the clock signal goes low, the output Q will latch (hold) the last value of the input D as shown in fig-b-

In a positive-edge-triggered flip-flop, the output changes with the positive edge of the clock

A latch is used commonly to interface output device when the mp sends an output, data are available on the data bus for only a few microseconds, and therefore, a latch is used to hold data for display.