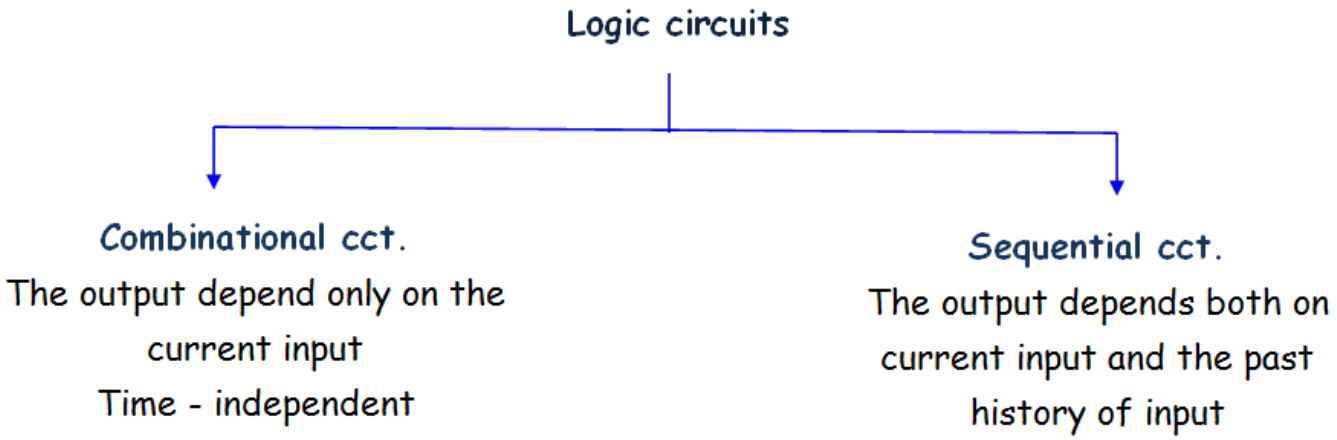
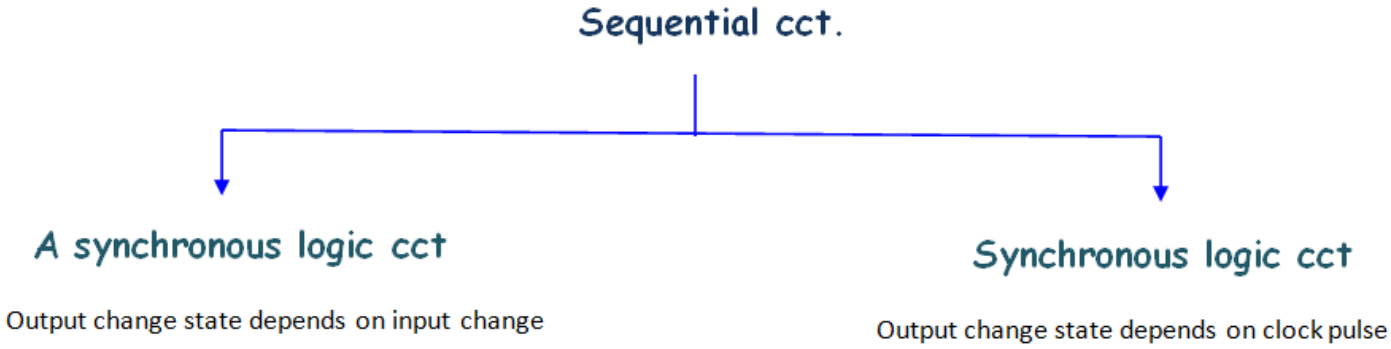
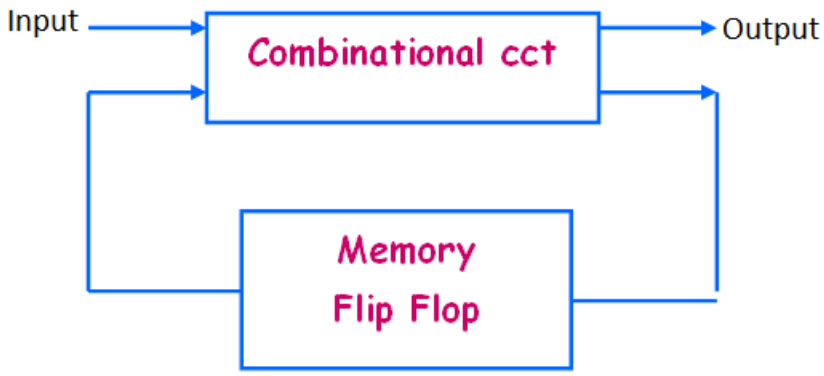
Sequential circuits:



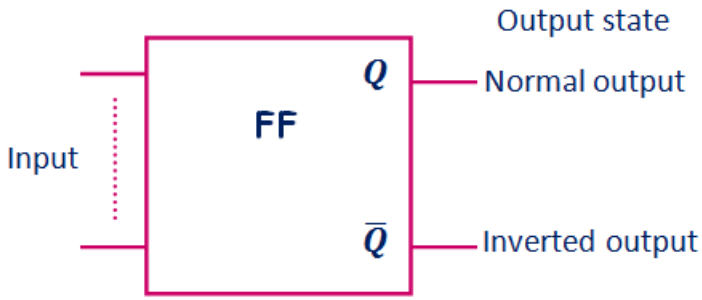


Most sequential system are based on element known a flip-flop (F.F.) memory element.

The sequential logic has state (memory) while combinational logic not. In other words, sequential logic is combinational logic with memory.



The flip flop is made up of assemble of logic gates even though a logic gates by itself has no storage capability, several can be connected together in way that permit information to be stored.



Output states:

1- $Q = 1$, $\bar{Q} = 0$

High or 1 state, also called set state

2- $Q = 0$, $\bar{Q} = 1$

Low or 0 state, also called reset or clear state

SR- Flip Flop:

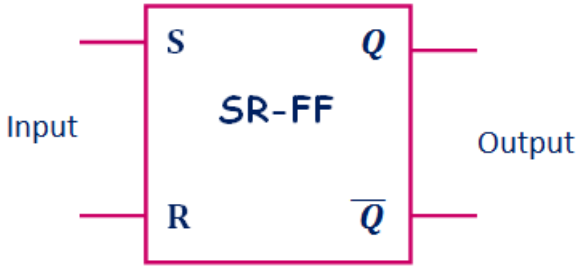
Also known as SR latch.

Can be consider as one of the most basic sequential logic circuit

It has two inputs:

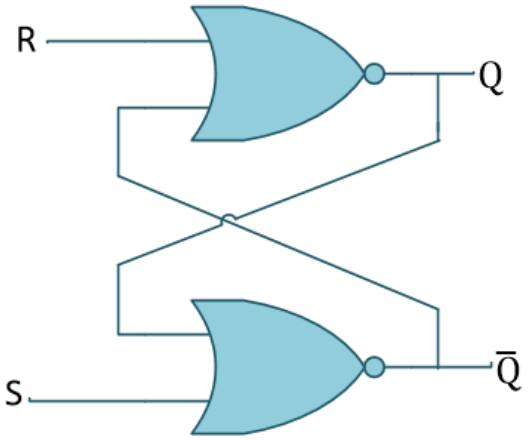
S which will SET the device , output = 1

R which will RESET the device, output = 0

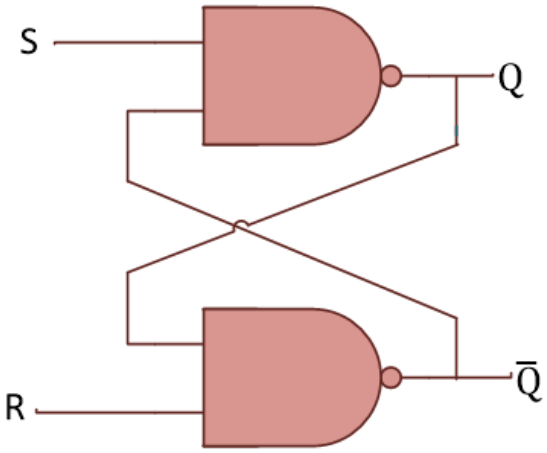


There are two types of SR latch

- Cross – coupled NOR
- Cross – coupled NAND

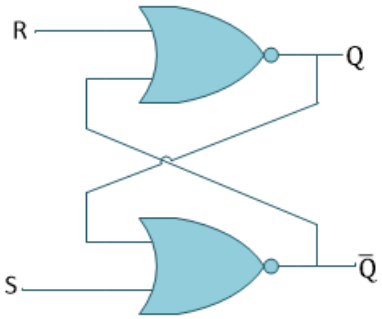


NOR-SR-FF

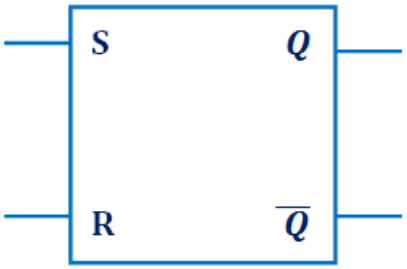


NAND-SR-FF

NOR – SR- Flip Flop:



NOR-SR-FF



Active high SR-FF

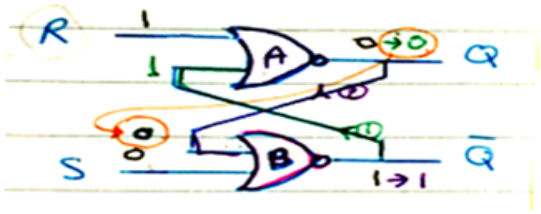
Active high indicates that a high (1) will activate the line

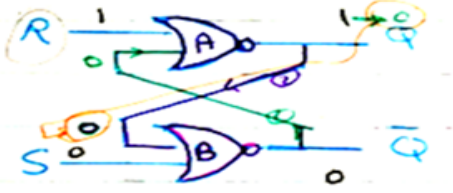
$S\ R$	Q_t	Q_{t+1}	
0 0	0	0	No change (NC)
0 0	1	1	
0 1	0	0	reset
0 1	1	0	
1 0	0	1	set
1 0	1	1	
1 1	0	X	invalid
1 1	1	X	

$S\ R$	Q_t
0 0	NC
0 1	0
1 0	1
1 1	Invalid

To understand the operation of SR it is instructive to trace through the logic signal when different values are placed on the S and R line, due to the feedback, this may require tracing the lines at least twice until the latch is in a stable state.

- **Reset condition:**

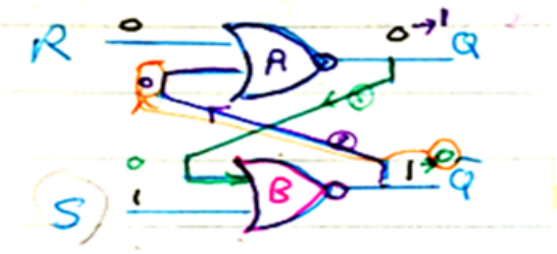


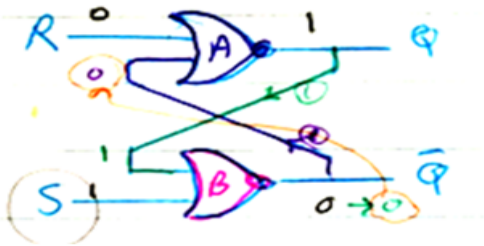


Initial $Q = 0$, $\bar{Q} = 1$
R = 1 , S = 0
Gate A i/p = 1 1
o/p = Q = 0
Gate B i/p = 0 0
o/p = $\bar{Q}$ = 1

Initial $Q = 1$, $\bar{Q} = 0$
R = 1 , S = 0
Gate A i/p = 1 0
o/p = Q = 0
Gate B i/p = 0 0
o/p = $\bar{Q}$ = 1

- **Set condition:**

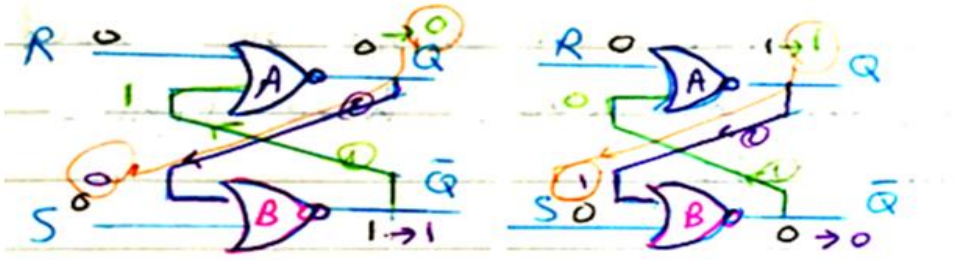




Initial $Q = 0$, $\bar{Q} = 1$
R = 0 , S = 1
Gate B i/p = 0 1
o/p = $\bar{Q}$ = 0
Gate A i/p = 0 0
o/p = Q = 1

Initial $Q = 1$, $\bar{Q} = 0$
R = 0 , S = 1
Gate B i/p = 1 1
o/p = $\bar{Q}$ = 0
Gate A i/p = 0 0
o/p = Q = 1

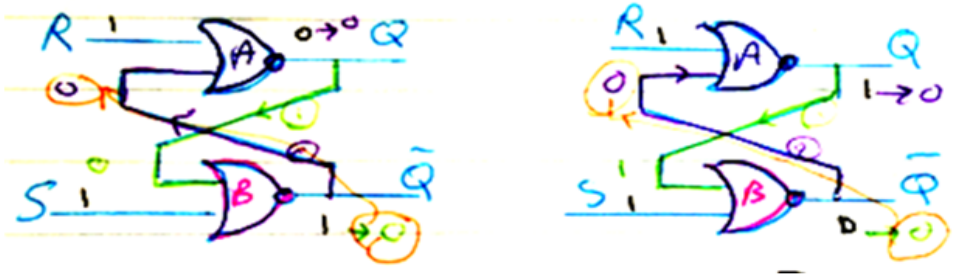
- **Hold condition (no change)**



Initial $Q = 0$, $\bar{Q} = 1$
R = 0 , S = 0
Gate A i/p = 0 1
o/p = Q = 0
Gate B i/p = 0 0
o/p = $\bar{Q}$ = 1

Initial $Q = 1$, $\bar{Q} = 0$
R = 0 , S = 0
Gate A i/p = 0 0
o/p = Q = 1
Gate B i/p = 0 1
o/p = $\bar{Q}$ = 0

- **Disallowed condition (invalid)**



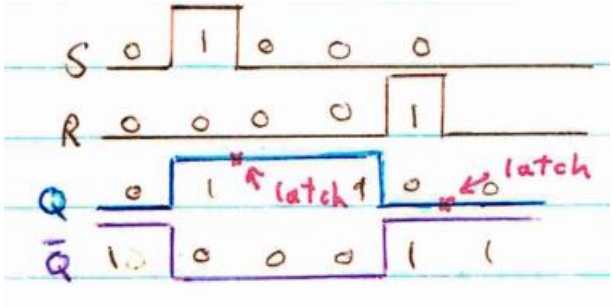
Initial $Q = 0$, $\bar{Q} = 1$
R = 1 , S = 1
Gate B i/p = 1 0
o/p = $\bar{Q}$ = 0
Gate A i/p = 1 0
o/p = Q = 0

Initial $Q = 1$, $\bar{Q} = 0$
R = 1 , S = 1
Gate B i/p = 1 1
o/p = $\bar{Q}$ = 0
Gate A i/p = 1 0
o/p = Q = 1

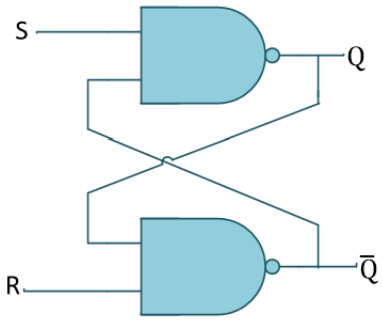
Note: Q and $\bar{Q}$ cannot both be 0 therefore R = 1 , S = 1 cannot be allowed to happen we avoid these inputs at all costs.

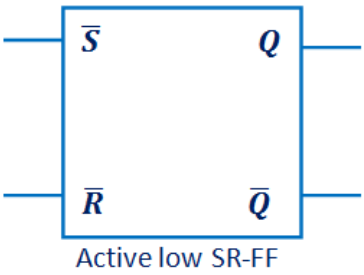
Time diagram :

Initial $Q = 0$



NAND-SR flip flop:



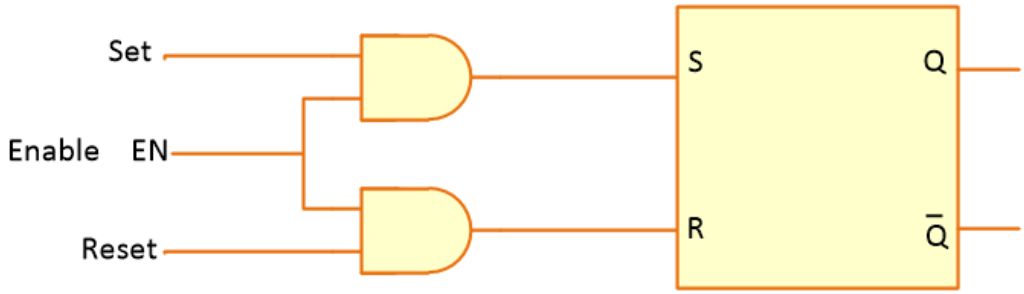


Active low SR-FF

Active low indicates that a low (0) will active the line

$S\ R$	Q
0 0	Invalid
0 1	1
1 0	0
1 1	NC

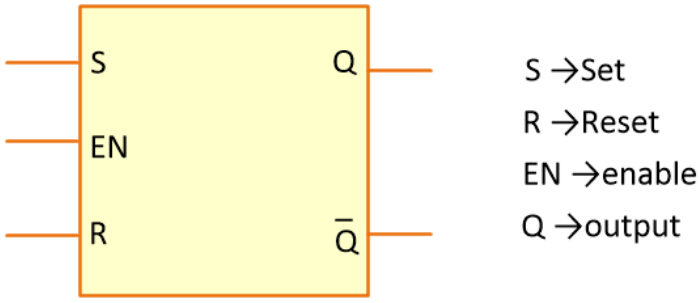
Gated SR latch:



The latch will operate normally when the enable is high (EN = 1)

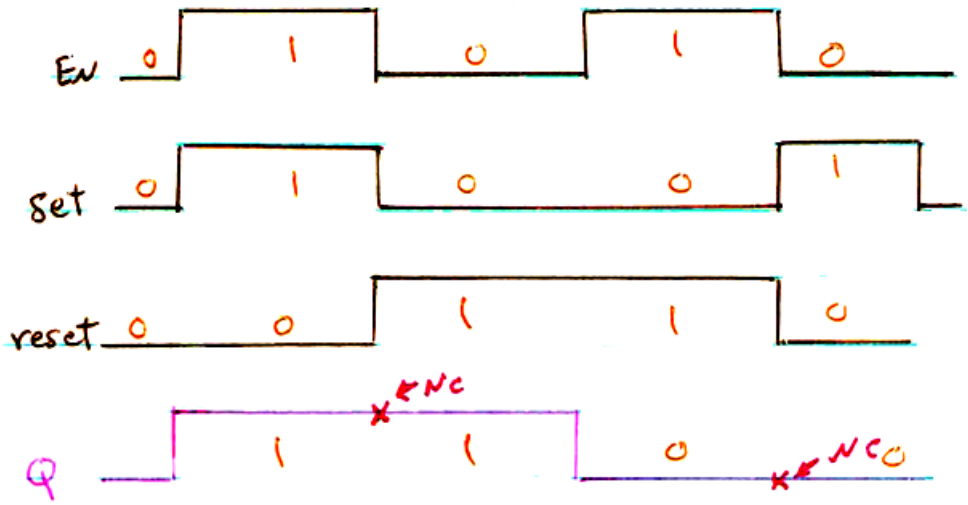
The latch will not respond when the enable is low (EN = 0)

EN	Set	Reset	SR	Q
0	0	0	00	NC
0	0	1	00	NC
0	1	0	00	NC
1	0	0	00	NC
1	0	1	01	0
1	1	0	10	1
1	1	1	11	Invalid



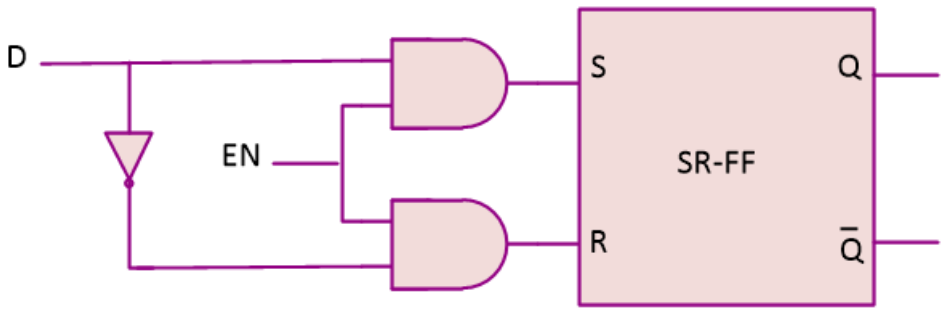
Gated SR-FF

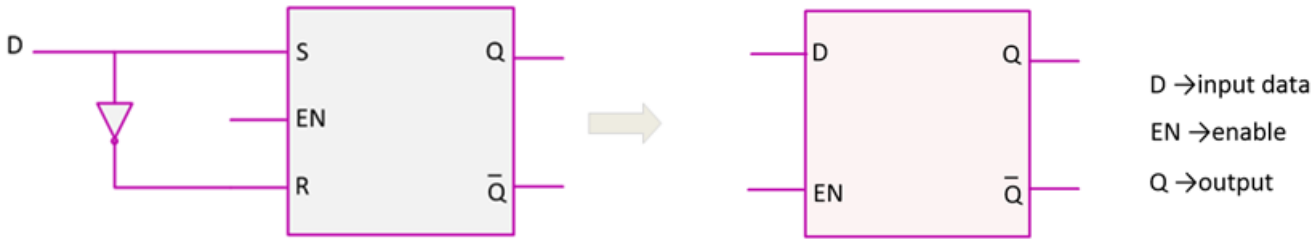
Time diagram:



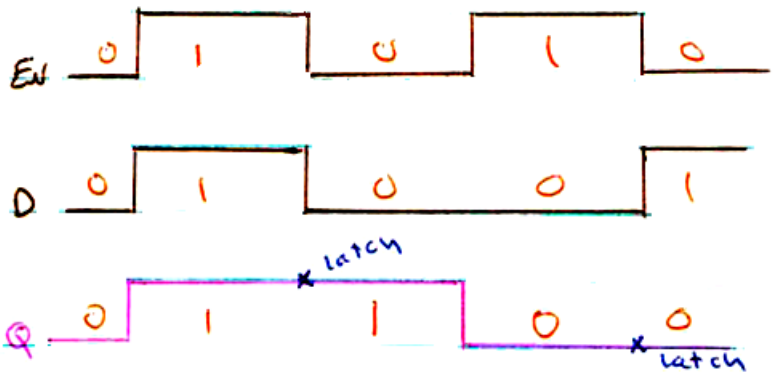
Gated D-latch:

A D-latch stands for data latch, A D-latch uses only one input to set and reset the latch this is achieved by placing a NOT gate between the S and R inputs.





EN	data	Q
0	0	NC
0	1	NC
1	0	0
1	1	1

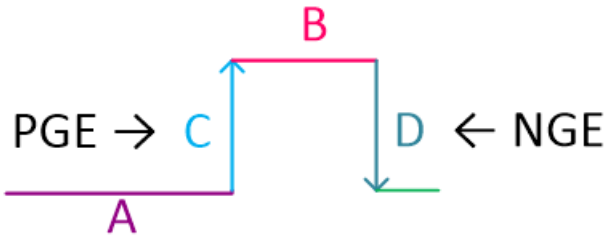


Note: the NOT gate guarantees that the unwanted RS = 11 does not occur.

Triggering and clocking :

A trigger is a control signal used to initiate an action
In the Gated latches, the trigger is enable line
Trigger can be of two forms:

1- Level triggers (high or low level)
2- Edge triggers (+ Ve or – Ve going transitions)

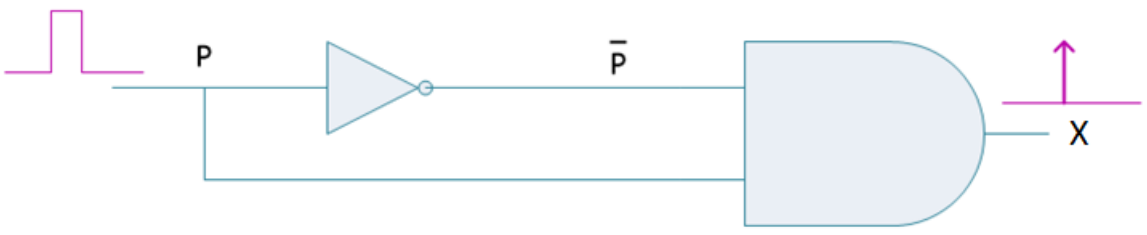


A: Low level
B: high level
C: positive Edge Low → high transition
D: negative Edge High → low transition

A level trigger means that an action is initiated on either a low or high level.
A edge trigger means that an action is initiated on either a positive or negative transition.
A clock : is a series of pulses (square wave) used to synchronies action.
Generally the trigger are taken from the edge of the clock.

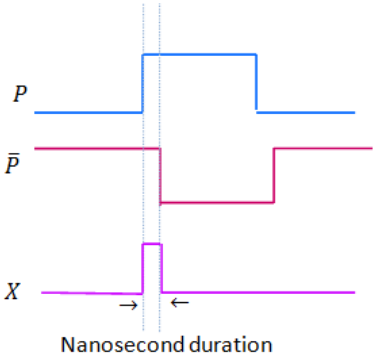
A method of Edge triggering detector:

The positive edge triggering circuit is given below



Propagation delay: is the time required for a digital signal to travel from the input of a logic gate to the output.

The propagation delay of inverter causes a delay of a few nanoseconds between P and $\bar{P}$, the AND gate translates this into a narrow pulse X of the order of a few nanoseconds in duration.



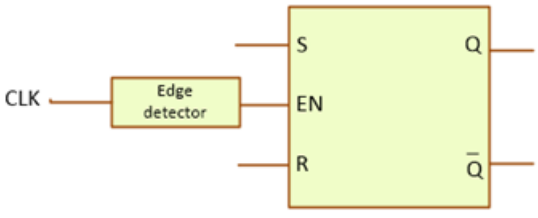
Pulse X is long enough to trigger a change in the state of the latches

Q/ how do you make a negative edge detector?

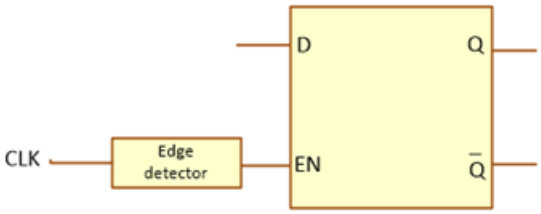
Ans: invert the pulse P before applying to the cct above or use NAND gate instead of AND gate.

Q/ how do you make edge triggered SR latch or D latch?

Ans: add the edge detector to the enable line.



Positive Edge triggered SR-FF

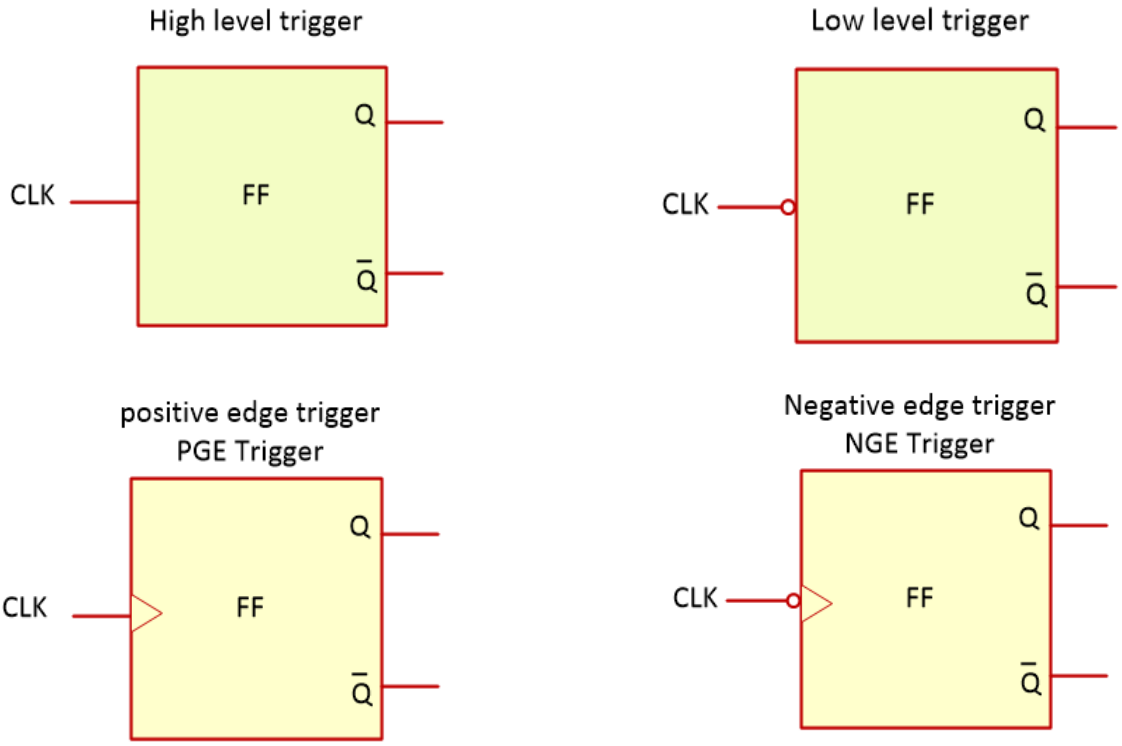


Positive Edge triggered D - FF

Edge	SR	Q
X	00	NC
↑	00	NC
↑	01	0
↑	10	1
↑	11	Invalid

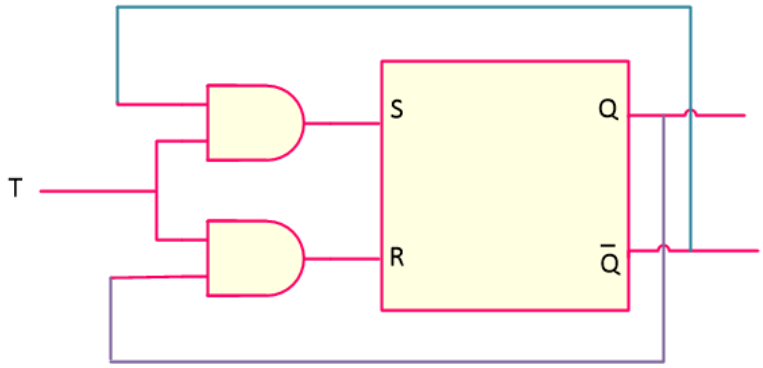
Don't care

Edge	D	Q
X	X	NC
↑	0	0
↑	1	1

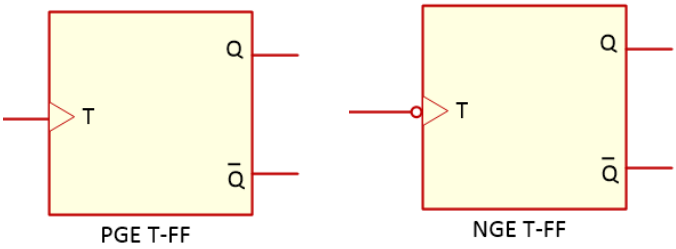


Toggle flip flop (T-FF):

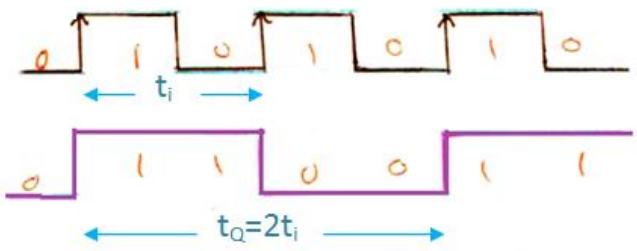
Toggle means to switch to the opposite state



T	Q_t	Q_{t+1}
0	0	0
0	1	1
1	0	1
1	1	0



Time diagram of PGE of T-FF:



A T-FF divided the frequency by two

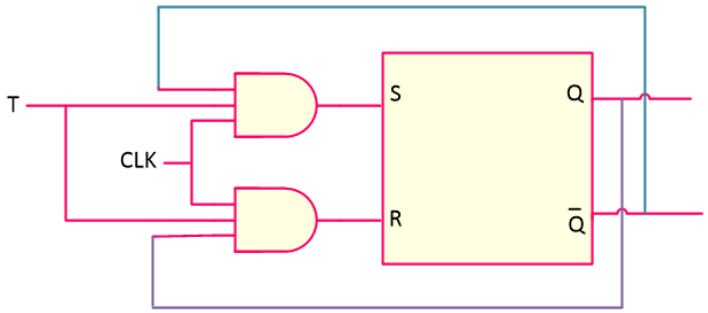
$t_Q = 2\ t_i$; t_Q = duration time of output

; t_i = duration time of input

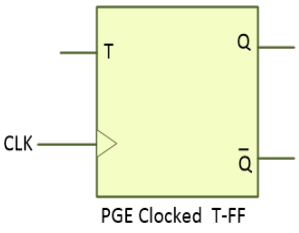
freq. = 1 / time

$f_Q = ½\ f_i$

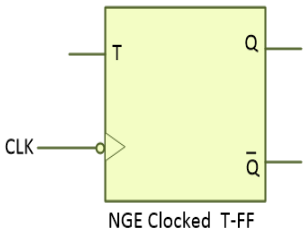
Clocked T-FF:



CLK	T	Q_t	Q_{t+1}
↑	0	0	0
↑	0	1	1
↑	1	0	1
↑	1	1	0

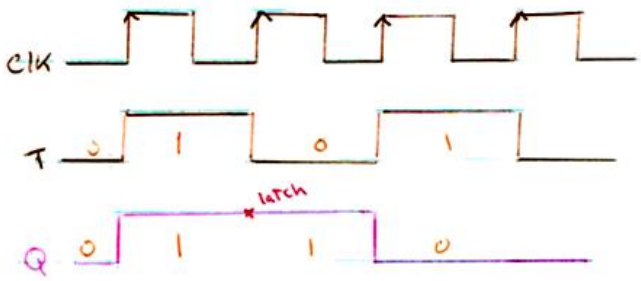


PGE Clocked T-FF



NGE Clocked T-FF

Time diagram PGE clocked T-FF

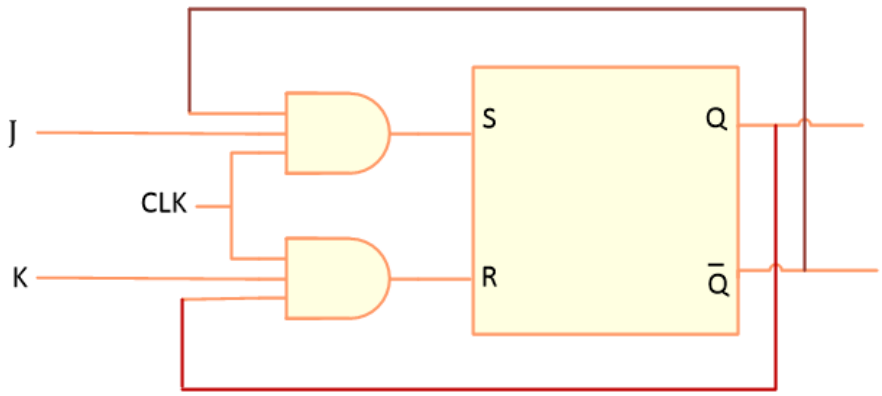


JK flip flop:

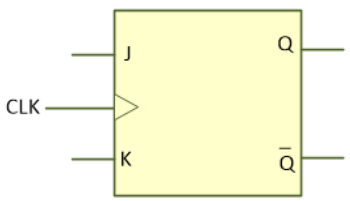
The JK-FF acts like SR-FF except that it does not have an invalid state

The J is equivalent to a set

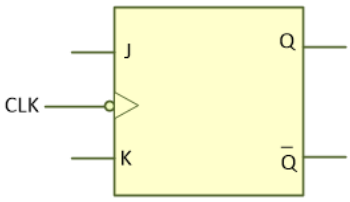
The K is equivalent to a reset



CLK	JK	Q
X	00	NC
↑	00	NC
↑	01	0
↑	10	1
↑	11	Toggle

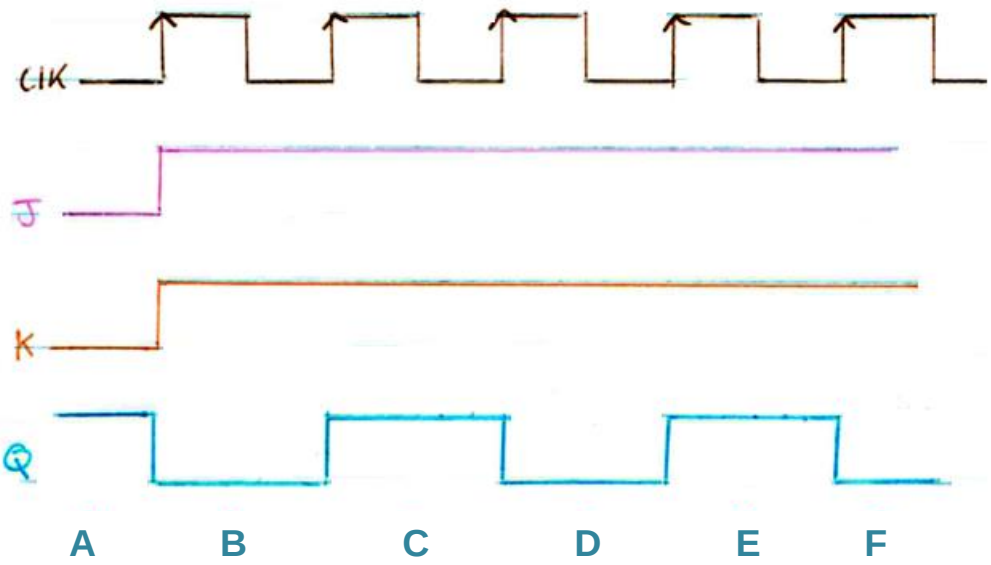


PGE-JK -FF



NGE-JK -FF

Note: the RS = 11 state has been replaced with a Toggle state.



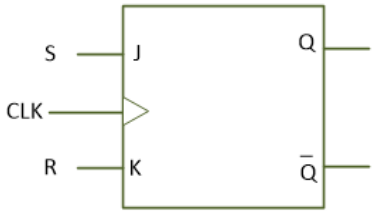
region	CLK	JK	Description	Q
A	0	00	Initial	1
B	↑	11	Toggle	0
C	↑	11	Toggle	1
D	↑	11	Toggle	0
E	↑	11	Toggle	1
F	↑	11	Toggle	0

Other types of flip flop from JK flip flop:

JK flip flop are widely used because of their versatility. They can be easily adapted for use as a SR-FF, D- FF and T-FF

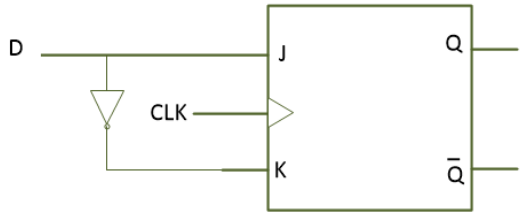
Edge Triggered SR-FF :

The SR-FF can be constructed out of a JK-FF by setting S = J and R = K



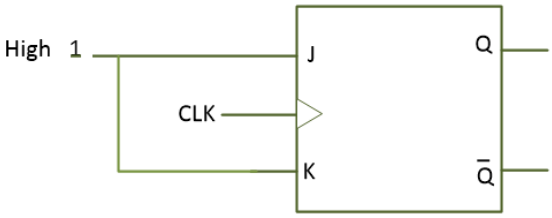
Edge Triggered D-FF :

The D-FF can be constructed out of a JK-FF by connecting an inverter between J and K



Edge Triggered T-FF :

The T-FF can be constructed out of a JK-FF by connecting J and K to high

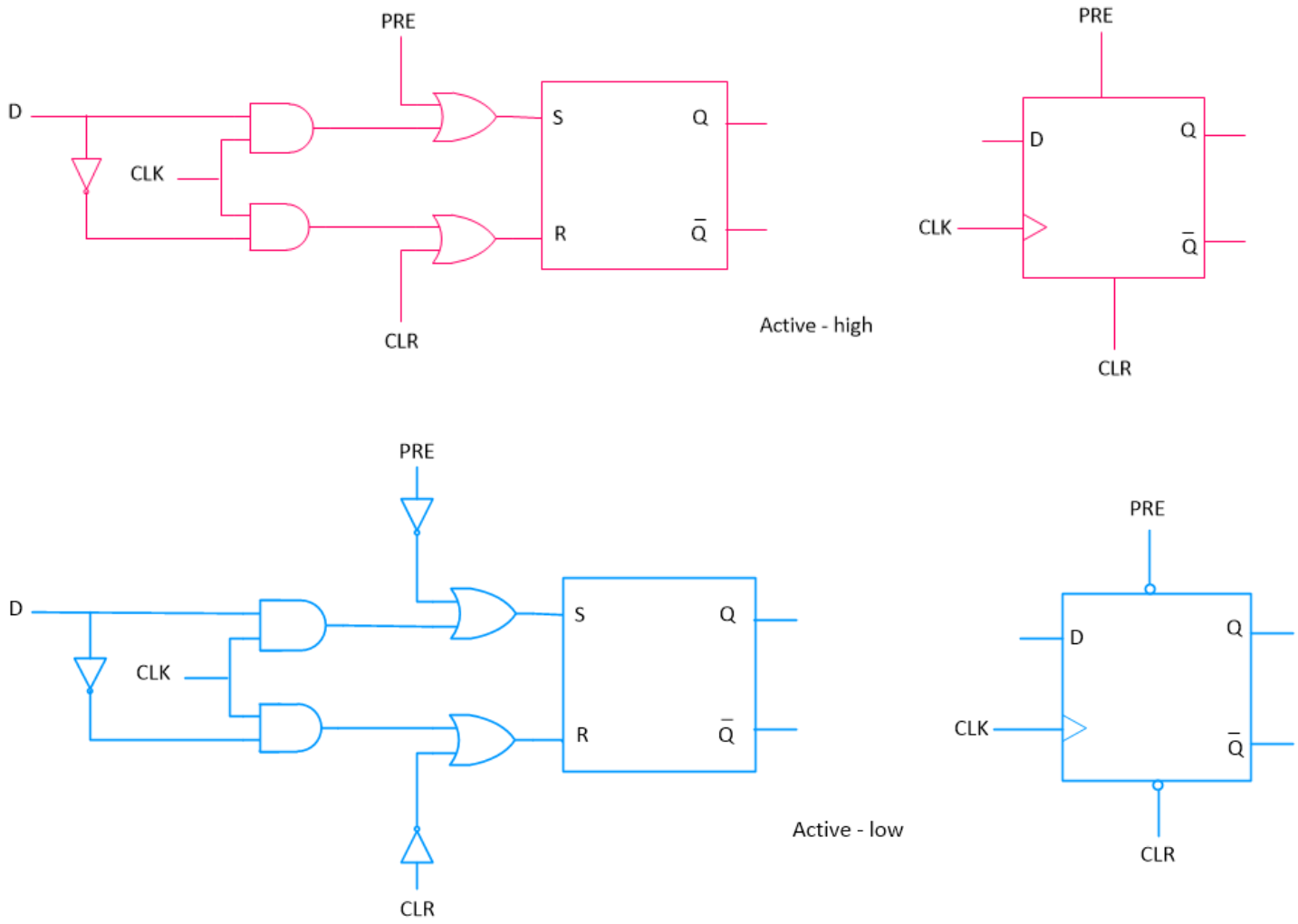


Preset and Clear inputs:

Preset and Clear inputs on a flip flop have control over the output Q and $\bar{Q}$ regardless of clock input status

The Preset (PRE) input drives the FF to a set state $Q = 1$

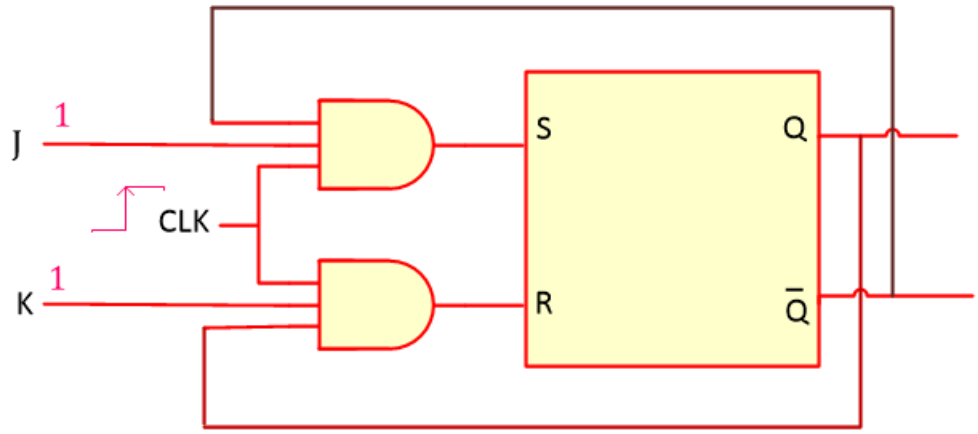
The Clear (CLR) input drives the FF to a set state $Q = 0$

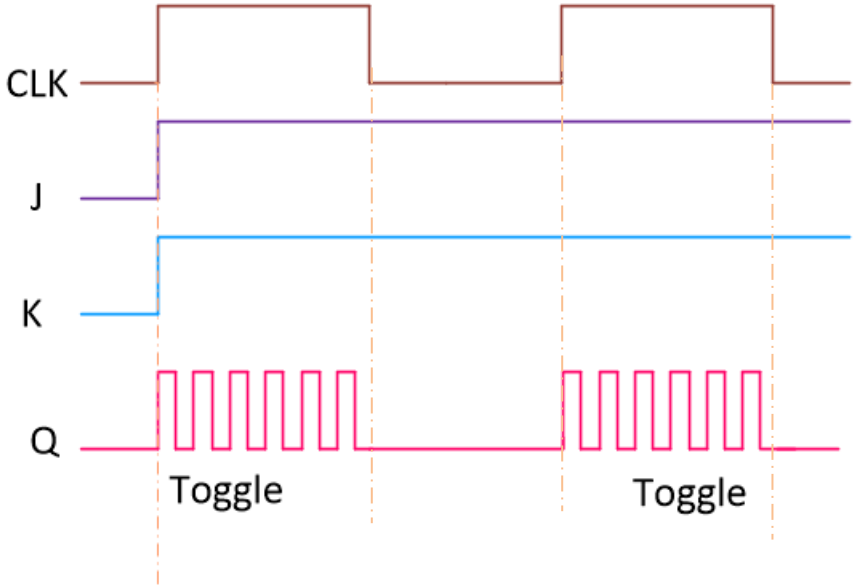


The Preset and Clear inputs find use when multiple FF are gonged to gether to perform a function on a multi-bit binary word, and a single line is needed to Set or Reset them all at once.

Race- around condition:

For JK flip flop when J=1 , K=1 , CLK =1 the output Q will toggle as long as CLK is high





Thus the output will be unstable creating a race-around condition

In order to avoid race-around condition

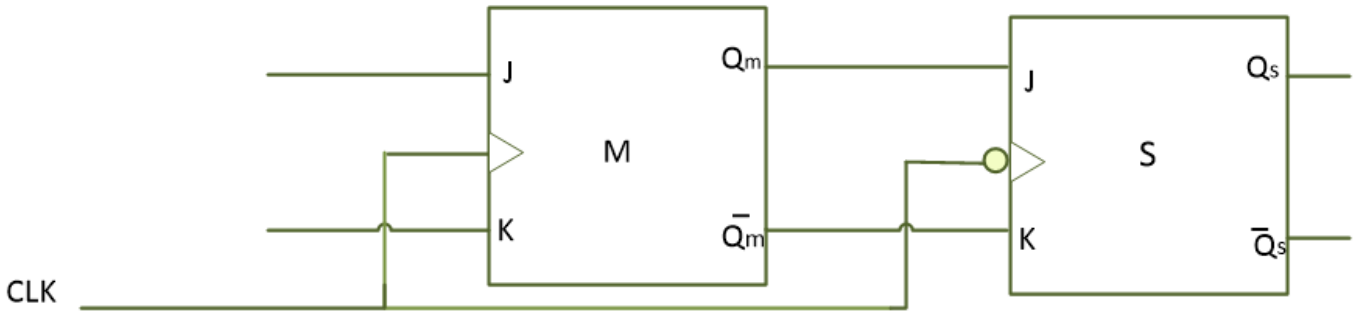
1- Use of Edge triggering

The output is effected only at the time of presence of edge

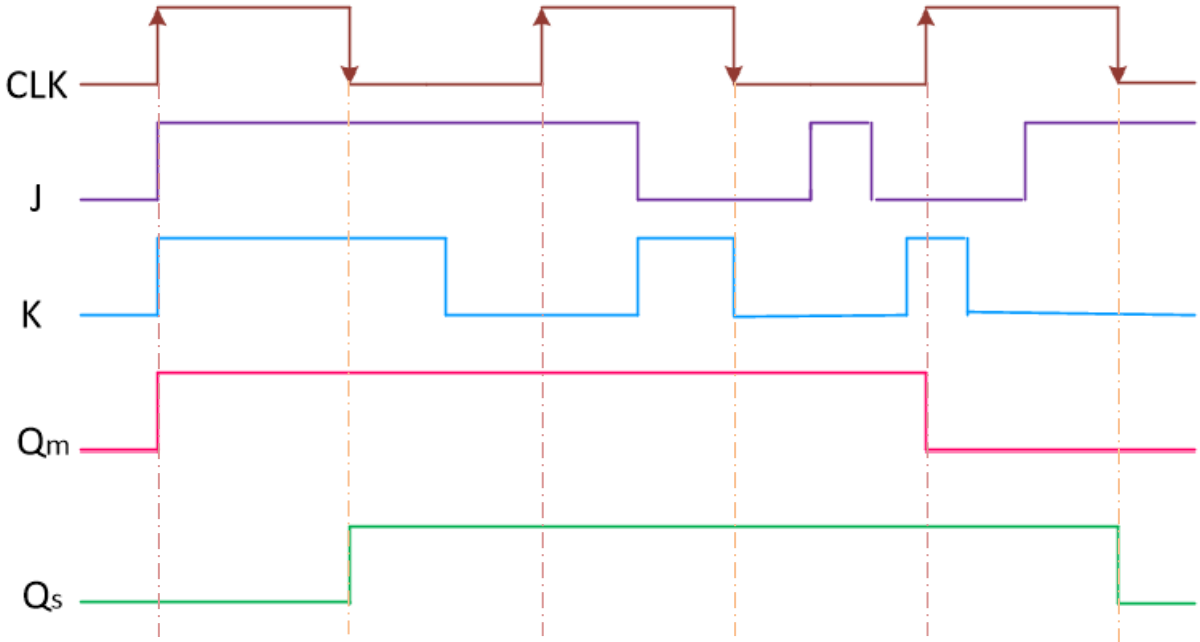
2- By using Master – Slave flip flop

It consists of two flip flop connected serially, the first FF called Master and the second is the Slave

In Master Slave flip flop inputs are fed at positive edge and output is available at the negative edge



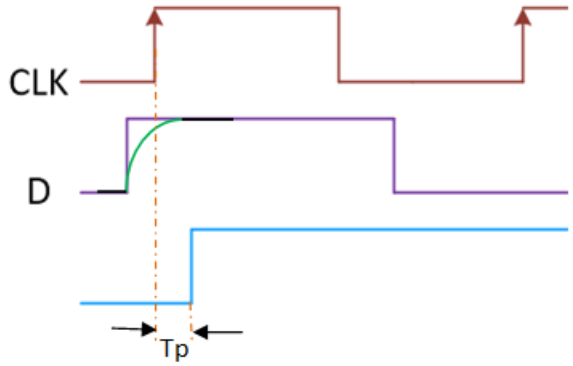
If the master's J and K input is high (1) it toggle on the positive clock edge and the slave then toggles on the negative clock edge, regardless of what the master does.



Flip Flop timing consideration:

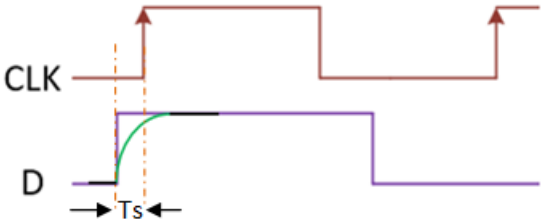
Propagation delay time (Tp):

Is amount of time it takes for the output of a gate or FF to change states after the input change. Tp ≈ in picosecond 10^{-12} or nanosecond 10^{-9}



Set up time Ts:

Is the minimum a mount of time that the data bit must be present before the clock edge hits. Ts ≈ nsec



Hold time T_H:

Is the minimum a mount of time the data bit must be present after clock edge arrives. T_H ≈ nsec