## Synchronous counter :

The synch. Counter is one in which all the flip flops in the counter are clocked at the same time by a common clock pulse.

### Design of synch. Counter:

| J K | Action of next clock pulse | |
|---|---|---|
| 0 0 | NC | $Q_{t+1} = Q_t$ |
| 0 1 | 0 | |
| 1 0 | 1 | |
| 1 1 | Toggle | $Q_{t+1} = \overline{Q_t}$ |

### Transition table:

| Present output $Q_t$ | Next output $Q_{t+1}$ | J | K | J | K |
|---|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 | X |
| | | 0 | 1 | | |
| 0 | 1 | 1 | 0 | 1 | X |
| | | 1 | 1 | | |
| 1 | 0 | 0 | 1 | X | 1 |
| | | 1 | 1 | | |
| 1 | 1 | 0 | 0 | X | 0 |
| | | 1 | 0 | | |

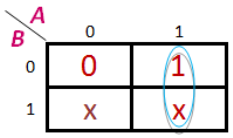
⇨

| $Q_t$ | $Q_{t+1}$ | J K |
|---|---|---|
| 0 | 0 | 0 X |
| 0 | 1 | 1 X |
| 1 | 0 | X 1 |
| 1 | 1 | X 0 |

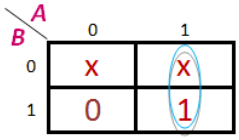
## 2- bit synch counter

| CLK | B A | $B_tA_t$ | $J_B\ K_B$ | $J_A\ K_A$ |
|---|---|---|---|---|
| 0 | 0 0 | 0 1 | 0 X | 1 X |
| 1 | 0 1 | 1 0 | 1 X | X 1 |
| 2 | 1 0 | 1 1 | X 0 | 1 X |
| 3 | 1 1 | 0 0 | X 1 | X 1 |

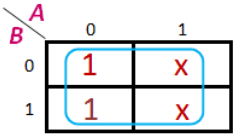
Using k-map:



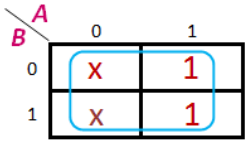

$J_B = A$



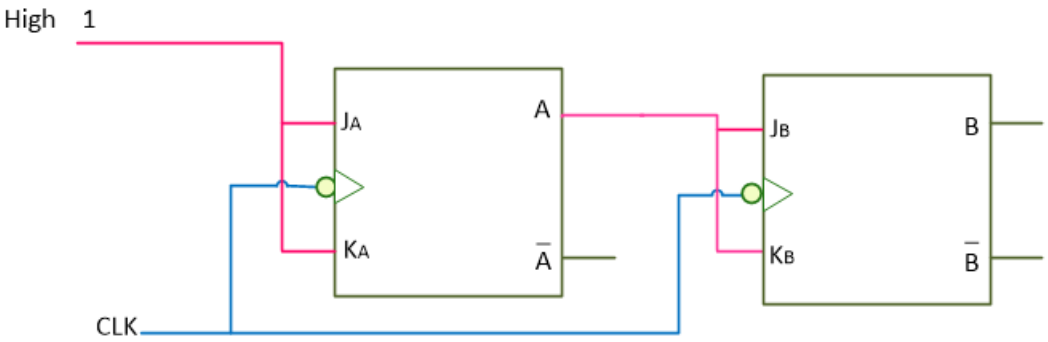

$K_B = A$

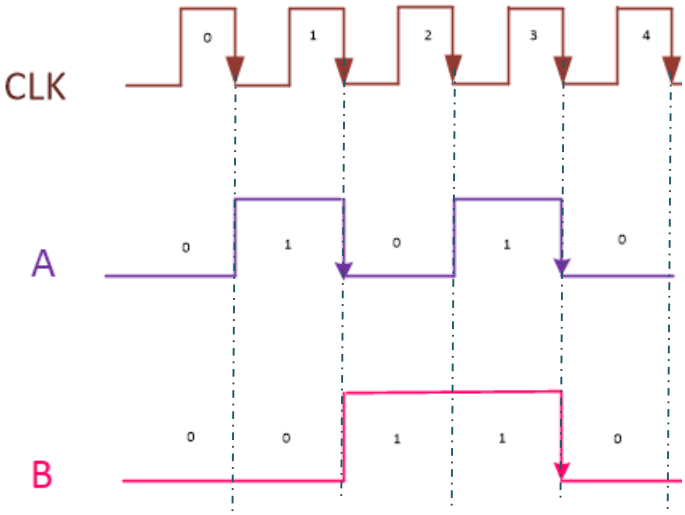



$J_A = 1$



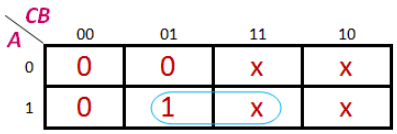

$K_A = 1$



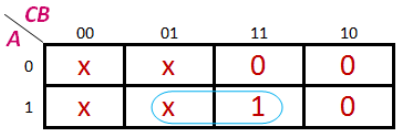



## 3-bit synch counter:

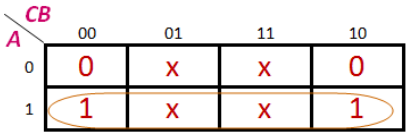
| C B A | $C_tB_tA_t$ | $J_C\ K_C$ | $J_B\ K_B$ | $J_A\ K_A$ |
|---|---|---|---|---|
| 0 0 0 | 0 0 1 | 0 X | 0 X | 1 X |
| 0 0 1 | 0 1 0 | 0 X | 1 X | X 1 |
| 0 1 0 | 0 1 1 | 0 X | X 0 | 1 X |
| 0 1 1 | 1 0 0 | 1 X | X 1 | X 1 |
| 1 0 0 | 1 0 1 | X 0 | 0 X | 1 X |
| 1 0 1 | 1 1 0 | X 0 | 1 X | X 1 |
| 1 1 0 | 1 1 1 | X 0 | X 0 | 1 X |
| 1 1 1 | 0 0 0 | X 1 | X 1 | X 1 |



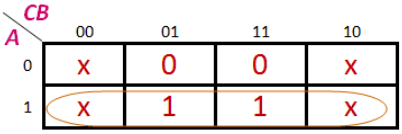

$J_C = BA$



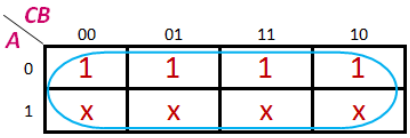

$K_C = BA$



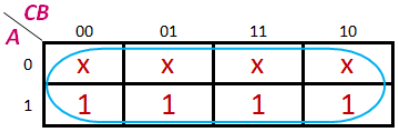

$J_B = A$



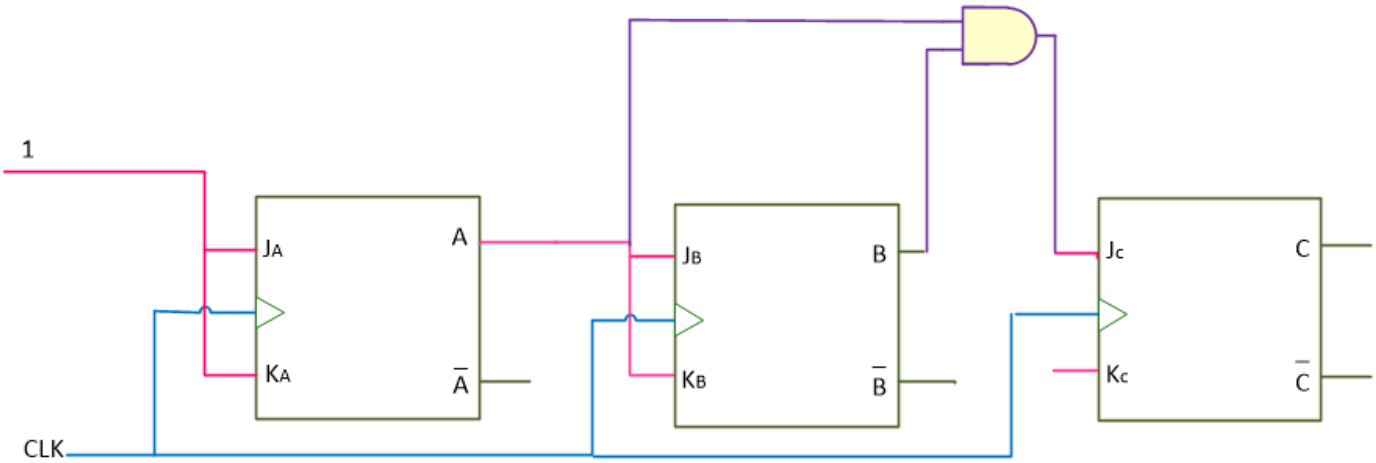

$K_B = A$

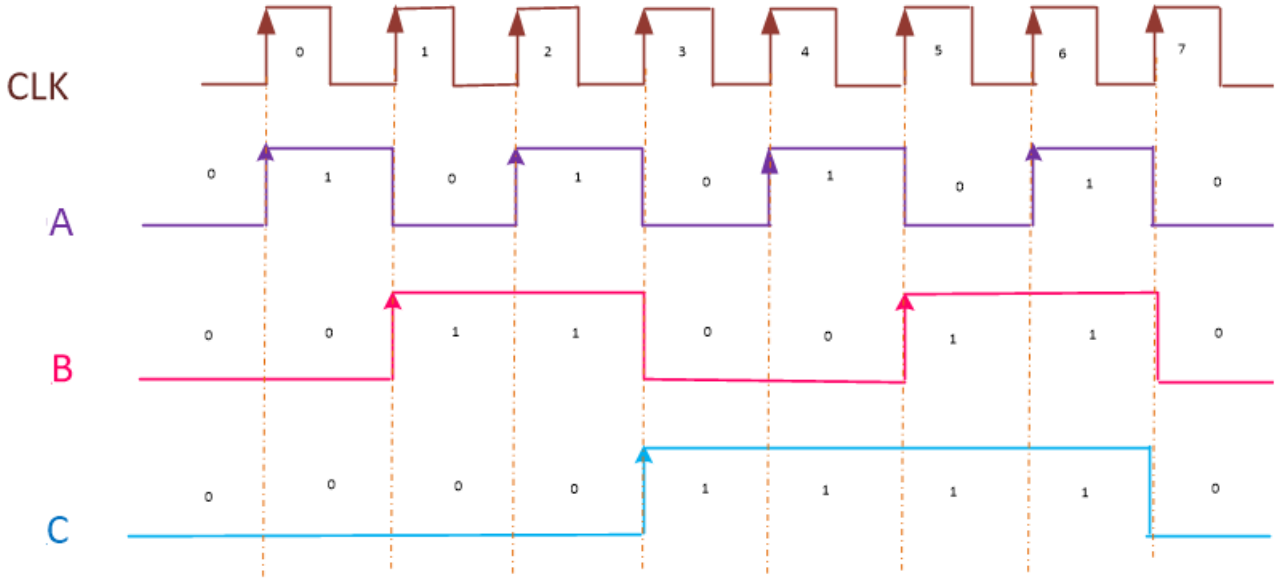



$J_A = 1$




$K_A = 1$

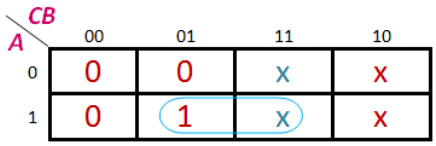

1
JA
A
KA
$\overline{A}$
JB
B
KB
$\overline{B}$
Jc
C
Kc
$\overline{C}$
CLK


CLK
A
B
C

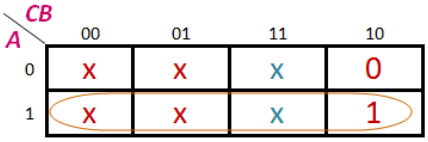
ex: design a divide-by – six up counter (synch.)

| CLK | C B A | $C_t B_t A_t$ | $J_C\ K_C$ | $J_B\ K_B$ | $J_A\ K_A$ |
|---|---|---|---|---|---|
| 0 | 0 0 0 | 0 0 1 | 0 X | 0 X | 1 X |
| 1 | 0 0 1 | 0 1 0 | 0 X | 1 X | X 1 |
| 2 | 0 1 0 | 0 1 1 | 0 X | X 0 | 1 X |
| 3 | 0 1 1 | 1 0 0 | 1 X | X 1 | X 1 |
| 4 | 1 0 0 | 1 0 1 | X 0 | 0 X | 1 X |
| 5 | 1 0 1 | 0 0 0 | X 1 | 0 X | X 1 |
| 6 | 0 0 0 | | | | |

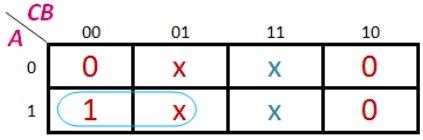
110 , 111 is skip , JK is don't care



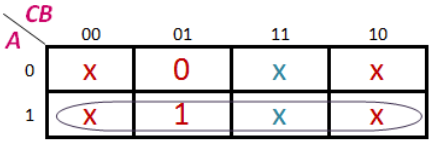

$J_C = BA$



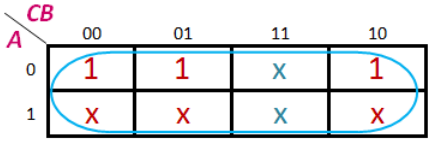

$K_C = A$



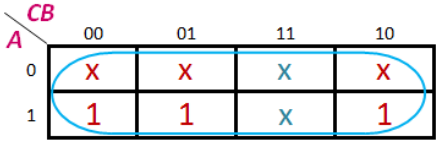

$J_B = A\bar{C}$



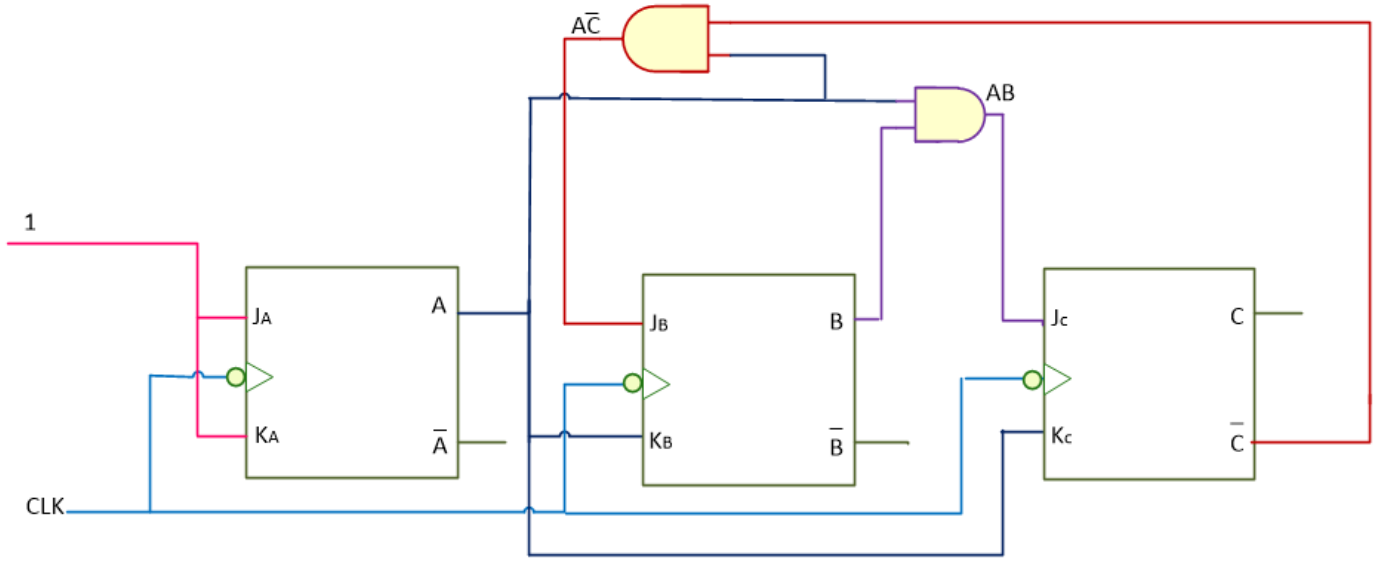

$K_B = A$

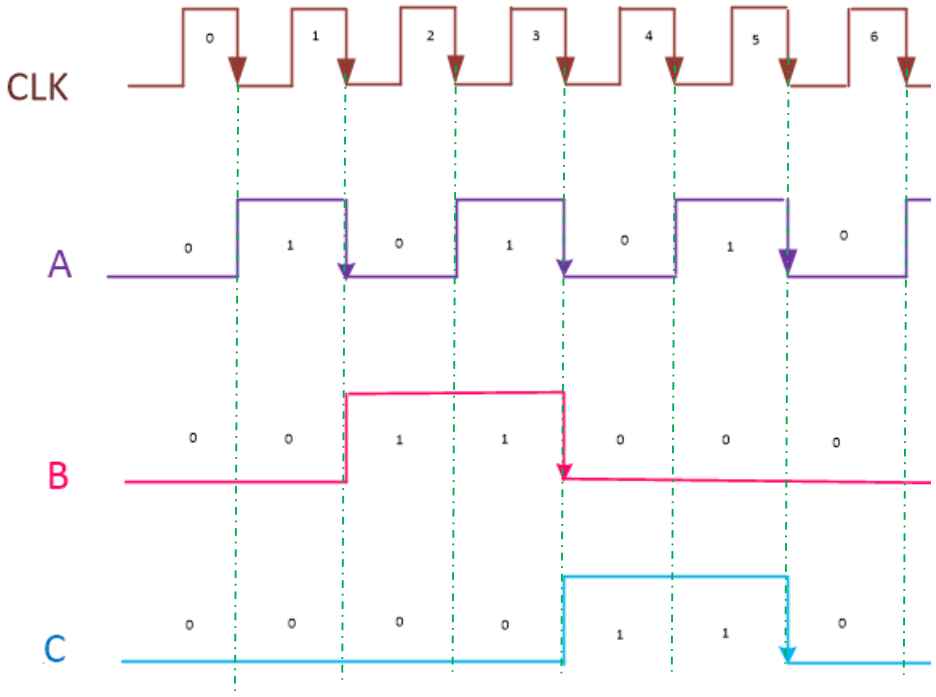



$J_A = 1$

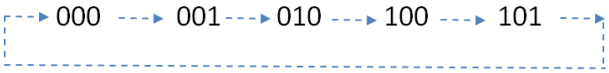



$K_A = 1$

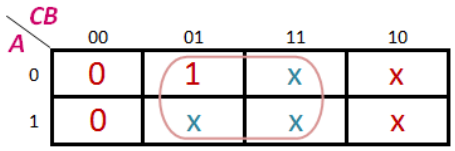

AC̄
AB
1
JA
A
KA
Ā
JB
B
KB
B̄
Jc
C
Kc
C̄
CLK


CLK
A
B
C
0
1
2
3
4
5
6

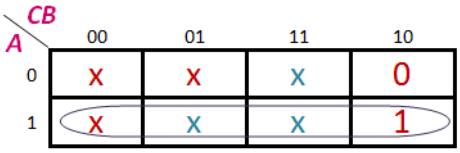
ex: design a synch. Counter that has a repeated sequence of five state as:



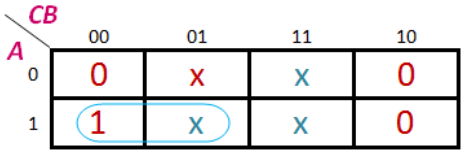

| CLK | C B A | $C_tB_tA_t$ | $J_C\ K_C$ | $J_B\ K_B$ | $J_A\ K_A$ |
|---|---|---|---|---|---|
| 0 | 0 0 0 | 0 0 1 | 0 X | 0 X | 1 X |
| 1 | 0 0 1 | 0 1 0 | 0 X | 1 X | X 1 |
| 2 | 0 1 0 | 1 0 0 | 1 X | X 1 | 0 X |
| 3 | 1 0 0 | 1 0 1 | X 0 | 0 X | 1 X |
| 4 | 1 0 1 | 0 0 0 | X 1 | 0 X | X 1 |
| 5 | 0 0 0 | | | | |



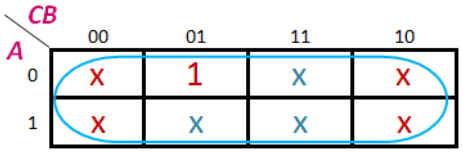

$J_C = B$



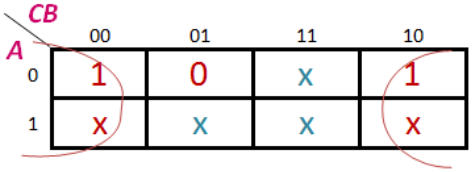

$K_C = A$



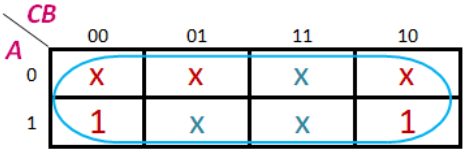

$J_B = A\bar{C}$



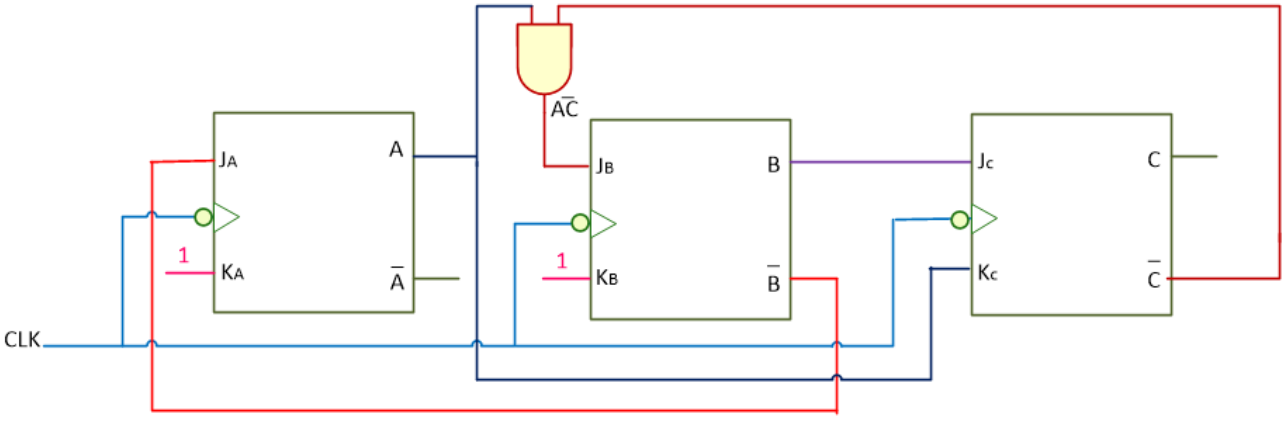

$K_B = 1$




$J_A = \bar{B}$

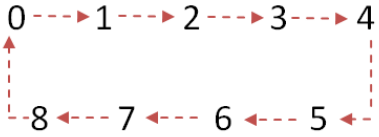



$K_A = 1$

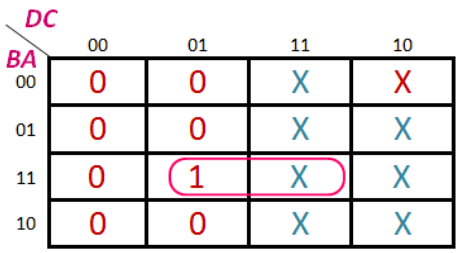


ex: design synch. Cct to count the first nine state of 8421 binary code

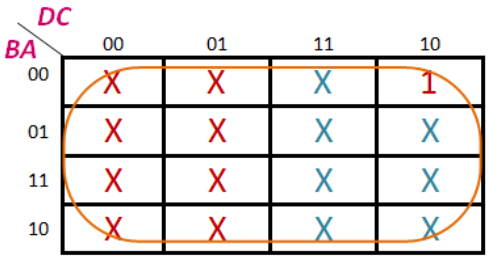
Investigate what happens if the counter goes into any of the cannot happen state




| DCBA | $D_tC_tB_tA_t$ | $J_D\,K_D$ | $J_C\,K_C$ | $J_B\,K_B$ | $J_A\,K_A$ |
|---|---|---|---|---|---|
| 0 0 0 0 | 0 0 0 1 | 0 X | 0 X | 0 X | 1 X |
| 0 0 0 1 | 0 0 1 0 | 0 X | 0 X | 1 X | X 1 |
| 0 0 1 0 | 0 0 1 1 | 0 X | 0 X | X 0 | 1 X |
| 0 0 1 1 | 0 1 0 0 | 0 X | 1 X | X 1 | X 1 |
| 0 1 0 0 | 0 1 0 1 | 0 X | X 0 | 0 X | 1 X |
| 0 1 0 1 | 0 1 1 0 | 0 X | X 0 | 1 X | X 1 |
| 0 1 1 0 | 0 1 1 1 | 0 X | X 0 | X 0 | 1 X |
| 0 1 1 1 | 1 0 0 0 | 1 X | X 1 | X 1 | X 1 |
| 1 0 0 0 | 0 0 0 0 | X 1 | 0 X | 0 X | 0 X |
| 1 0 0 1 | X X XX | X X | X X | X X | X X |
| 1 0 1 0 | X X XX | X X | X X | X X | X X |
| 1 0 1 1 | X X XX | X X | X X | X X | X X |
| 1 1 0 0 | X X XX | X X | X X | X X | X X |
| 1 1 0 1 | X X XX | X X | X X | X X | X X |
| 1 1 1 0 | X X XX | X X | X X | X X | X X |
| 1 1 1 1 | X X XX | X X | X X | X X | X X |




$J_D = ABC$




$K_D = 1$

| BA \ DC | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | 0 | X | X | 0 |
| 01 | 0 | X | X | X |
| 11 | 1 | X | X | X |
| 10 | 0 | X | X | X |

$$J_C = AB$$

| BA \ DC | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | X | 0 | X | X |
| 01 | X | 0 | X | X |
| 11 | X | 1 | X | X |
| 10 | X | 0 | X | X |

$$K_C = AB$$

| BA \ DC | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | 0 | 0 | X | 0 |
| 01 | 1 | 1 | X | X |
| 11 | X | X | X | X |
| 10 | X | X | X | X |

$$J_B = A$$

| BA \ DC | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | X | X | X | X |
| 01 | X | X | X | X |
| 11 | 1 | 1 | X | X |
| 10 | 0 | 0 | X | X |

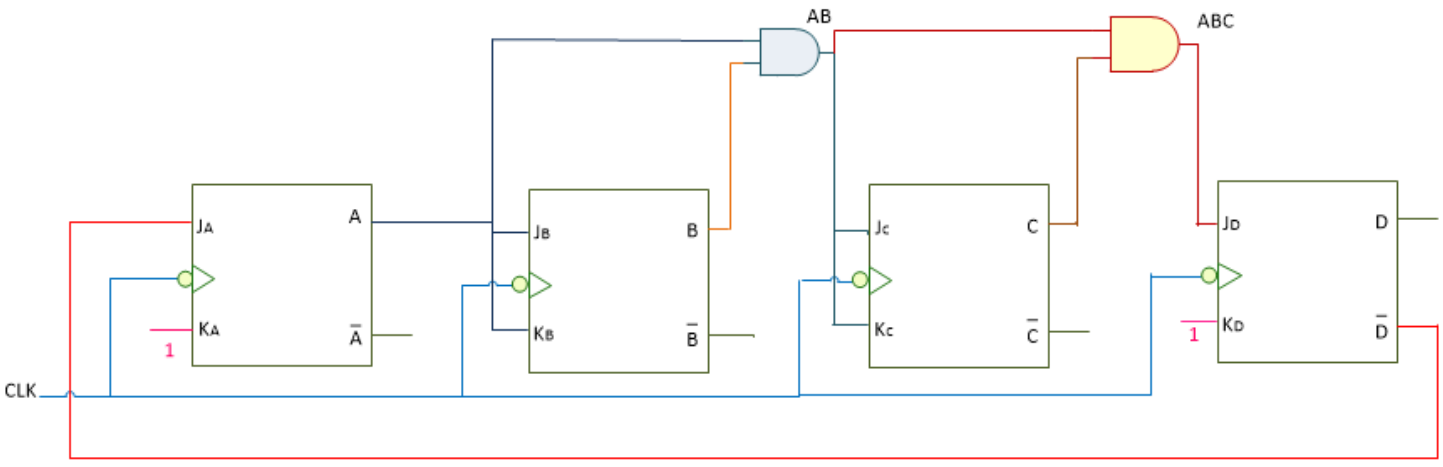
$$K_B = A$$

| BA \ DC | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | 1 | 1 | X | 0 |
| 01 | X | X | X | X |
| 11 | X | X | X | X |
| 10 | 1 | 1 | X | X |

$$J_A = \overline{D}$$

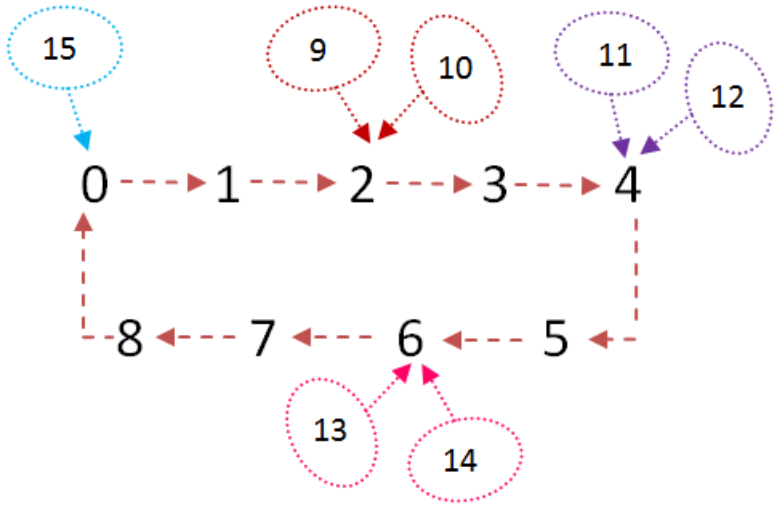
| BA \ DC | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | X | X | X | X |
| 01 | 1 | 1 | X | X |
| 11 | 1 | 1 | X | X |
| 10 | X | X | X | X |

$$K_A = 1$$



Preset

| D C B A | $J_D\ K_D$ | $J_C\ K_C$ | $J_B\ K_B$ | $J_A\ K_A$ | $D_tC_tB_tA_t$ |
|---|---|---|---|---|---|
| 1 0 0 1 | 0 1 | 0 0 | 1 1 | 0 1 | 0 0 1 0 |
| 1 0 1 0 | 0 1 | 0 0 | 0 0 | 0 1 | 0 0 1 0 |
| 1 0 1 1 | 0 1 | 1 1 | 1 1 | 0 1 | 0 1 0 0 |
| 1 1 0 0 | 0 1 | 0 0 | 0 0 | 0 1 | 0 1 0 0 |
| 1 1 0 1 | 0 1 | 0 0 | 1 1 | 0 1 | 0 1 1 0 |
| 1 1 1 0 | 0 1 | 0 0 | 0 0 | 0 1 | 0 1 1 0 |
| 1 1 1 1 | 1 1 | 1 1 | 1 1 | 0 1 | 0 0 0 0 |

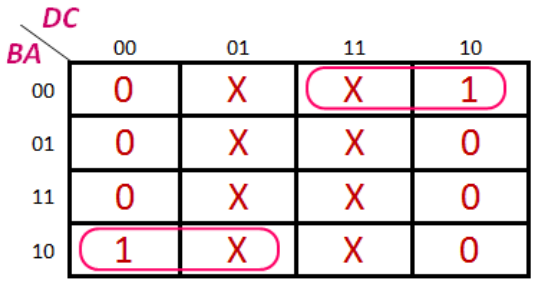


## Synch. Up – down counter:

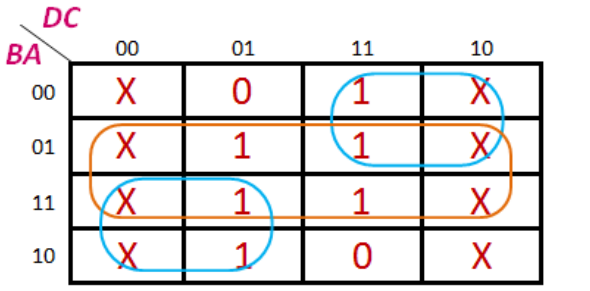
ex: design synch. Counter using JK flip flop and any extra logic cct's needed to count the sequence 0,2,4,6 when the control line D= 0, and count the sequence 6,4,2,0 when the control line D= 1

If the cct falls into any disallowed states, it should go always to the reset state.

| D | C B A | $C_t B_t A_t$ | $J_C\ K_C$ | $J_B\ K_B$ | $J_A\ K_A$ |
|---|---|---|---|---|---|
| 0 | 0 0 0 | 0 1 0 | 0 X | 1 X | 0 X |
| 0 | 0 1 0 | 1 0 0 | 1 X | X 1 | 0 X |
| 0 | 1 0 0 | 1 1 0 | X 0 | 1 X | 0 X |
| 0 | 1 1 0 | 0 0 0 | X 1 | X 1 | 0 X |
| 0 | 0 0 1 | 0 0 0 | 0 X | 0 X | X 1 |
| 0 | 0 1 1 | 0 0 0 | 0 X | X 1 | X 1 |
| 0 | 1 0 1 | 0 0 0 | X 1 | 0 X | X 1 |
| 0 | 1 1 1 | 0 0 0 | X 1 | X 1 | X 1 |
| 1 | 1 1 0 | 1 0 0 | X 0 | X 1 | 0 X |
| 1 | 1 0 0 | 0 1 0 | X 1 | 1 X | 0 X |
| 1 | 0 1 0 | 0 0 0 | 0 X | X 1 | 0 X |
| 1 | 0 0 0 | 1 1 0 | 1 X | 1 X | 0 X |
| 1 | 0 0 1 | 0 0 0 | 0 X | 0 X | X 1 |
| 1 | 0 1 1 | 0 0 0 | 0 X | X 1 | X 1 |
| 1 | 1 0 1 | 0 0 0 | X 1 | 0 X | X 1 |
| 1 | 1 1 1 | 0 0 0 | X 1 | X 1 | X 1 |




$J_C = \bar{A}\bar{B}D + \bar{A}B\bar{D} = \bar{A}(B \oplus D)$




$K_C = A + B\bar{D} + \bar{B}D = A + (B \oplus D)$

| DC / BA | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | 1 | 1 | 1 | 1 |
| 01 | 0 | 0 | 0 | 0 |
| 11 | X | X | X | X |
| 10 | X | X | X | X |

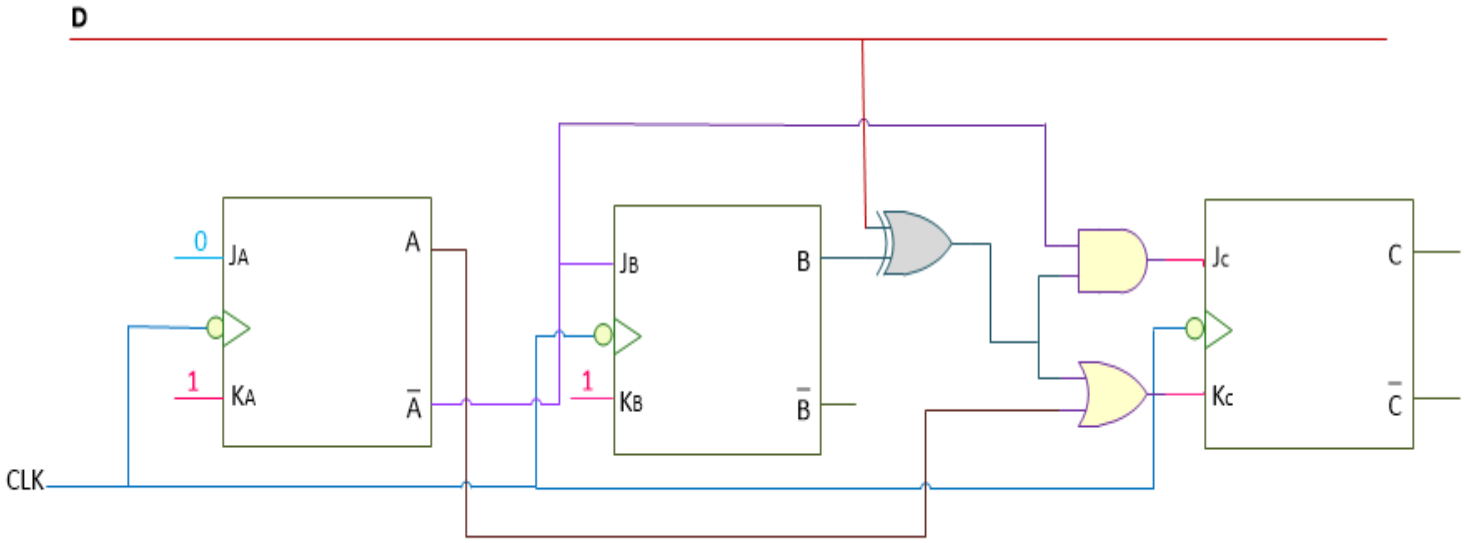
$J_B = \overline{A}$

$K_B = 1$

| DC / BA | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 00 | 0 | 0 | 0 | 0 |
| 01 | X | X | X | X |
| 11 | X | X | X | X |
| 10 | 0 | 0 | 0 | 0 |

$J_A = 0$

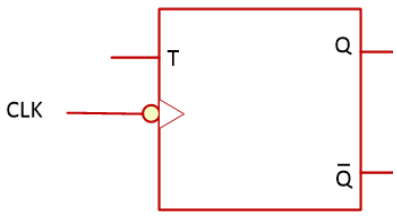
$K_A = 1$




## Synch. Counter using T flip flop:

### Transition table

| $Q$ | $Q_t$ | $T$ |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |




| $T$ | $Q$ | $Q_t$ |
|---|---|---|
| 0 | 0 | 0 |
| 0 | 1 | 1 |
| 1 | 0 | 1 |
| 1 | 1 | 0 |

$T = Q + Q_t \quad ; \quad Q_t = Q + T$

ex: design mod 8 synch. Counter using T flip flop

| C B A | $C_tB_tA_t$ | $T_C$ | $T_B$ | $T_A$ |
|---|---|---|---|---|
| 0 0 0 | 0 0 1 | 0 | 0 | 1 |
| 0 0 1 | 0 1 0 | 0 | 1 | 1 |
| 0 1 0 | 0 1 1 | 0 | 0 | 1 |
| 0 1 1 | 1 0 0 | 1 | 1 | 1 |
| 1 0 0 | 1 0 1 | 0 | 0 | 1 |
| 1 0 1 | 1 1 0 | 0 | 1 | 1 |
| 1 1 0 | 1 1 1 | 0 | 0 | 1 |
| 1 1 1 | 0 0 0 | 1 | 1 | 1 |

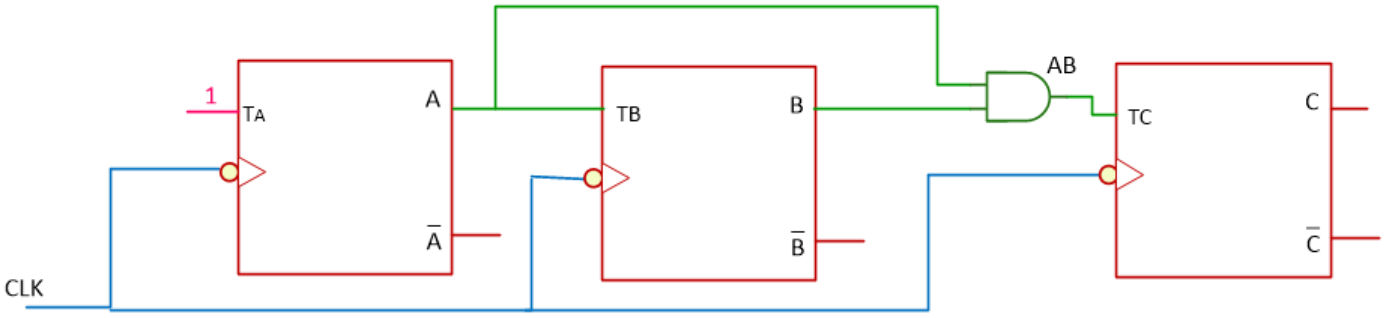
$$T_A = 1$$

| A \ CB | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 1 | 1 | 1 | 1 | 1 |

$T_B = A$

| A \ CB | 00 | 01 | 11 | 10 |
|---|---|---|---|---|
| 0 | 0 | 0 | 0 | 0 |
| 1 | 0 | 1 | 1 | 0 |

$T_C = AB$




## H.W

1- design a mod 4 up – down parallel counter using control line Z

Z = 0 up counter , Z = 1 down counter.

2- design synch. Divided by six up counter arranged so that any transition from unused state end at the first used state.