Counter:

A counter is a sequential cct. Used for counting pulses. It's a group of flip flop with a clock signal applied

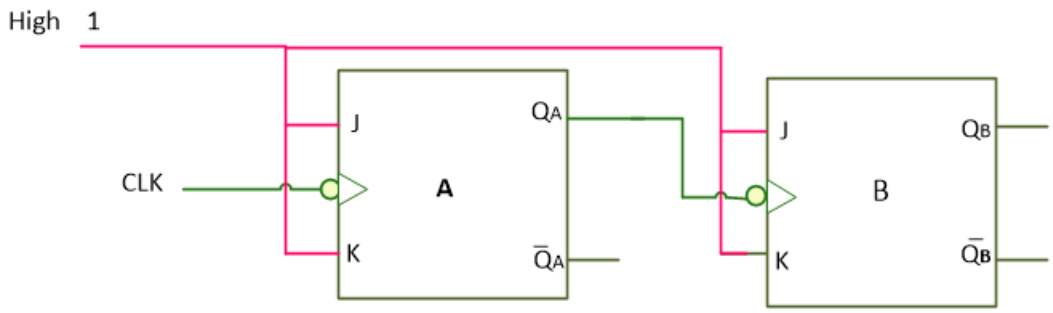
Counter type:

1- Asynchronous counter
2- Synchronous counter

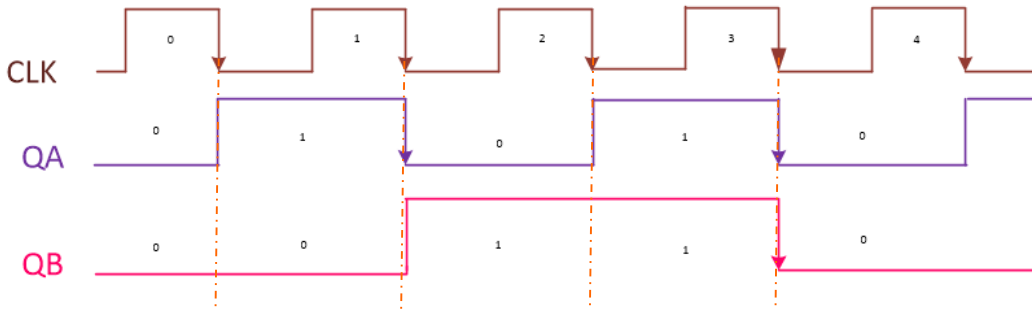
Asynchronous counter:

In which only the first Flip flop is clocked by the external clock. All subsequent flip flops are clocked by the output of the preceding flip flop.

2-bit Asynch. Up counter:

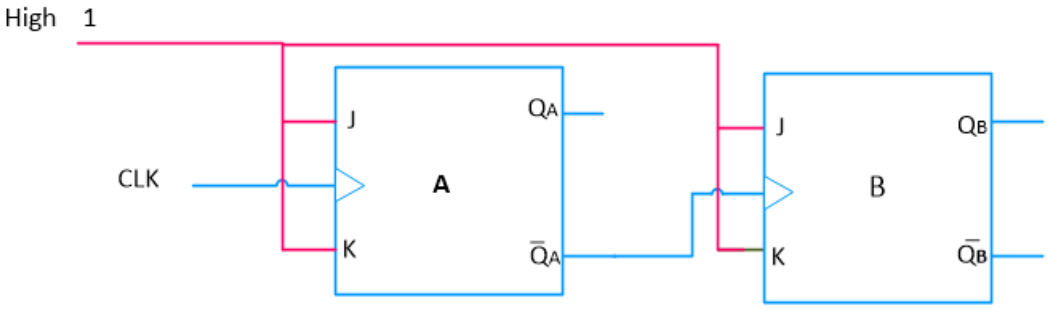


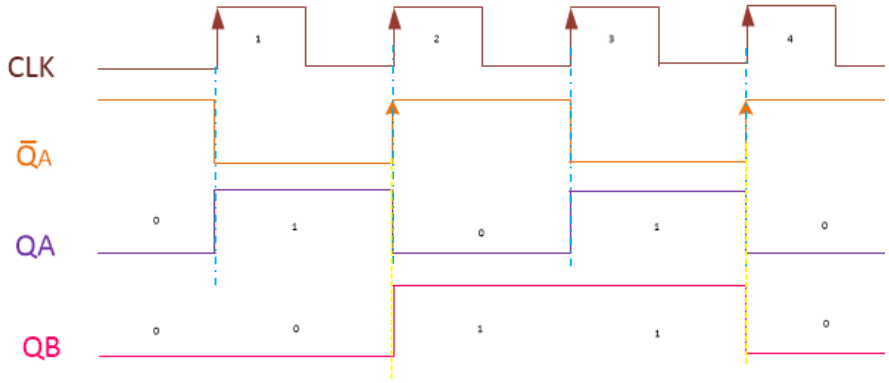
The FF's are NGE-JK , both FF's are initially reset, flip flop A toggles on the negative-going transition of each clock pulse, the QA clocked flip flop B , so each time QA makes a high to low transition flip flop B toggles.



QBQA	CLK
0 0	initial
0 1	1
1 0	2
1 1	3
0 0	4 recycle

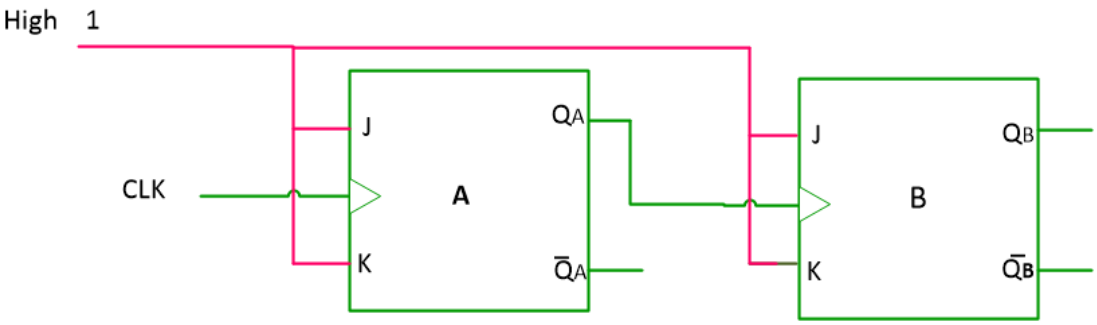
2-bit Asynch. Up counter using PGE trigger:

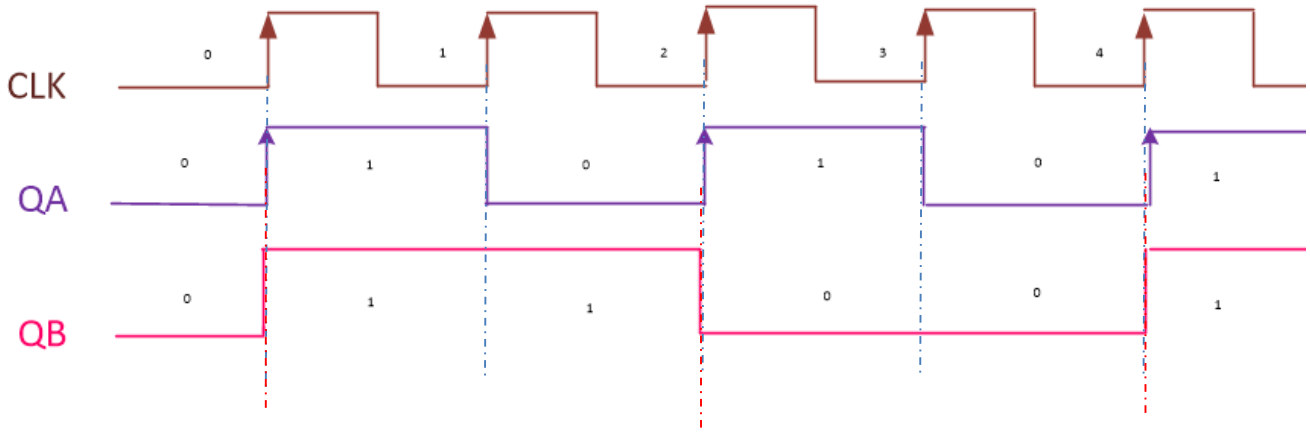




QBQA	CLK
0 0	initial
0 1	1
1 0	2
1 1	3
0 0	4 recycle

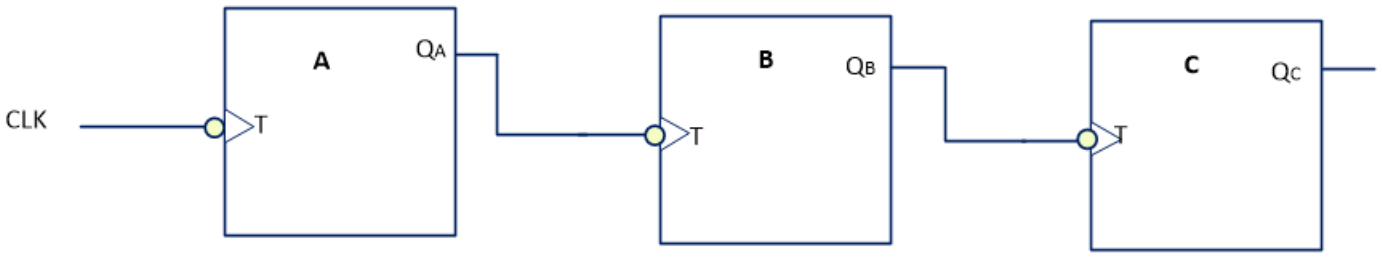
2-bit Asynch. down counter:

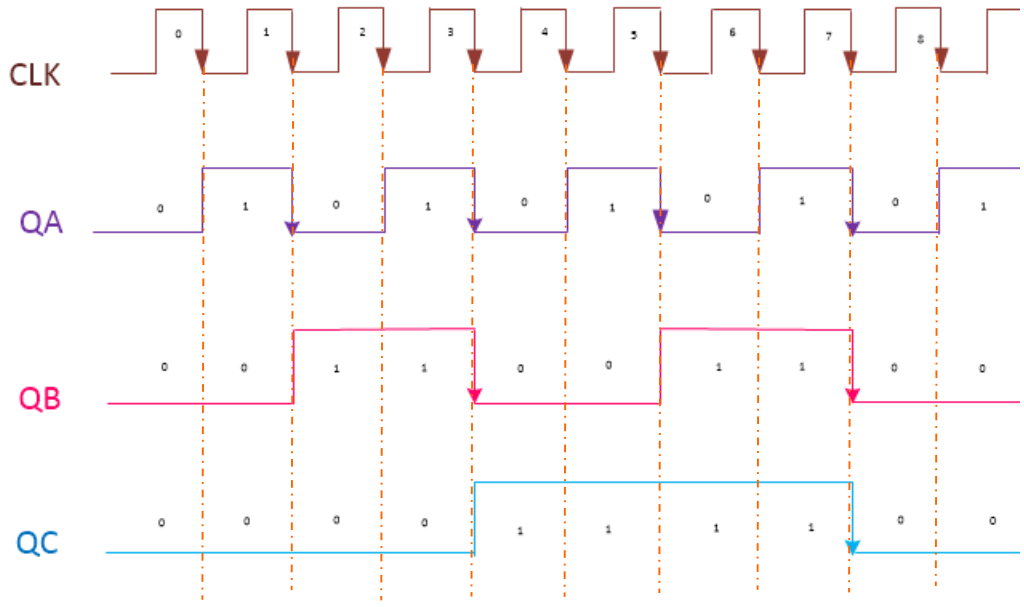




Q_BQ_A	CLK
0 0	initial
1 1	1
1 0	2
0 1	3
0 0	4
1 1	recycle

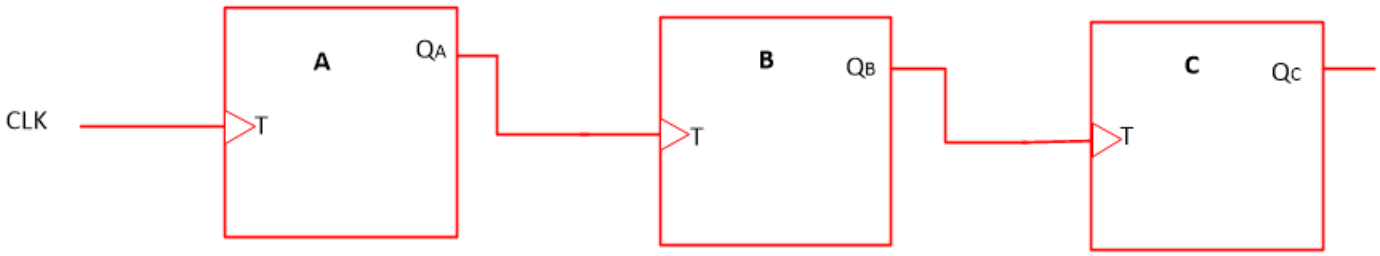
3-bit Asynch. Up counter:

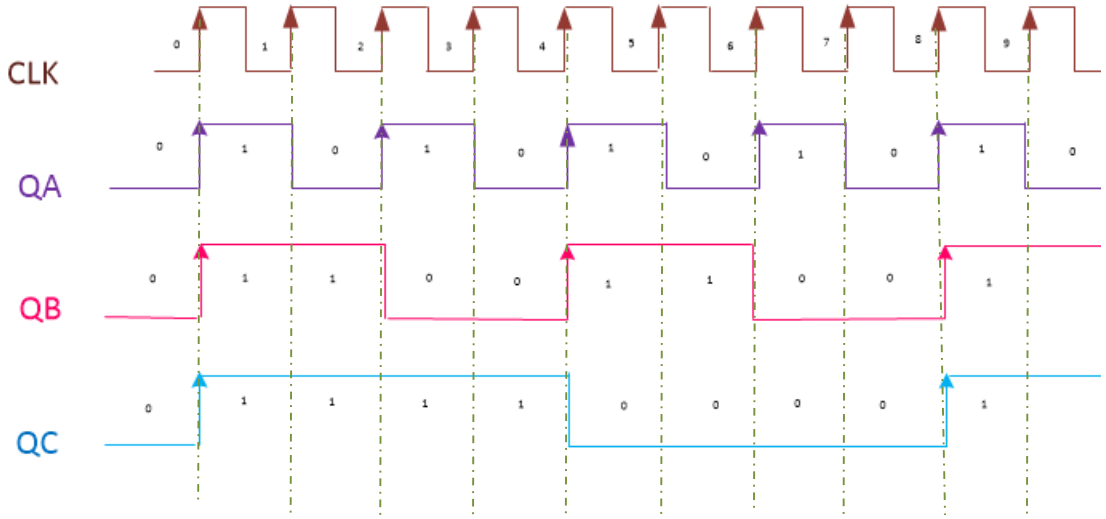




QCQBQA	CLK
0 0 0	initial
0 0 1	1
0 1 0	2
0 1 1	3
1 0 0	4
1 0 1	5
1 1 0	6
1 1 1	7
0 0 0	8 recycle

3-bit Asynch. down counter:





QCQBQA	CLK
0 0 0	initial
1 1 1	1
1 1 0	2
1 0 1	3
1 0 0	4
0 1 1	5
0 1 0	6
0 0 1	7
0 0 0	8
1 1 1	recycle

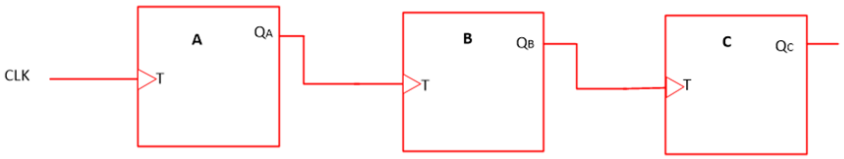
Note: a counter with n flip flop can have 2^n states, the number of states in a counter is known as it mod (Modula) number, thus 2-bit counter is a mod-4 counter, the max number the counter counts is 2^n-1 .

ex: n=3 ; n = number of flip flop

Number of state = $2^3 = 8$

So it's mod 8

Max number count = 2^3-1 = 7



$2^n \geq x$

Mod **x**

count	QCQBQA	state
0	0 0 0	1
1	0 0 1	2
2	0 1 0	3
3	0 1 1	4
4	1 0 0	5
5	1 0 1	6
6	1 1 0	7
7	1 1 1	8

Note: A mod **x** counter may also described as a divide by **x** counter, the most significant flip flop produces one pulse for every **x** pulses at the clock input of the lest significant flip flop. The output frequency is equal to the input frequency divided by **x** number of mod **x**

$$F_{output} = \frac{F_{input}}{x}$$

ex: mod 8 counter with clock freq. = 24 KHz

The output freq.= $\frac{\mathbf{24KHZ}}{\mathbf{8}}$ = 3KHz

Note: due to the propagation delay for each flip flop in a counter the max delay in a counter must be less than the period of the clock pulse

$t_{p\ total} < t_{clk}$

ex: a 4-bit asynch. Counter have 4-FF, each FF has propagation delay for 10 nsec. Determine the total propagation delay time, also determine the max clock freq. at which the counter can be operated.

Sol: the total propagation delay $t_{p\ total}$ = 4 x 10 nsec

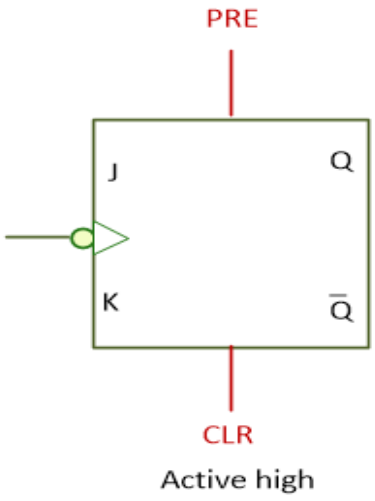
$$t_{p\ total} = 40 \text{ nsec}$$

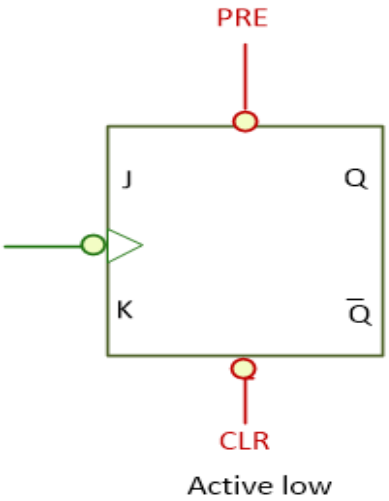
the max clock freq. is

$F_{max} = 1/ t_{p\ total} = 1/40\text{nsec} = 25 \text{ MHz}$

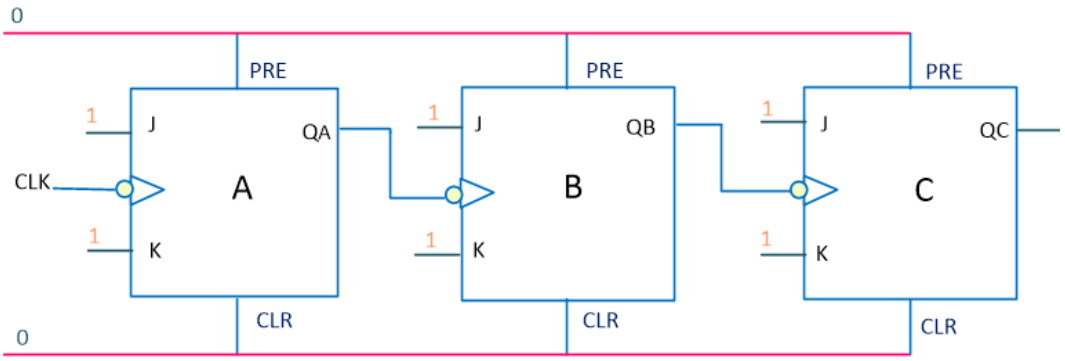
The counter should be operated below this freq. to avoid problem due to the propagation delay.

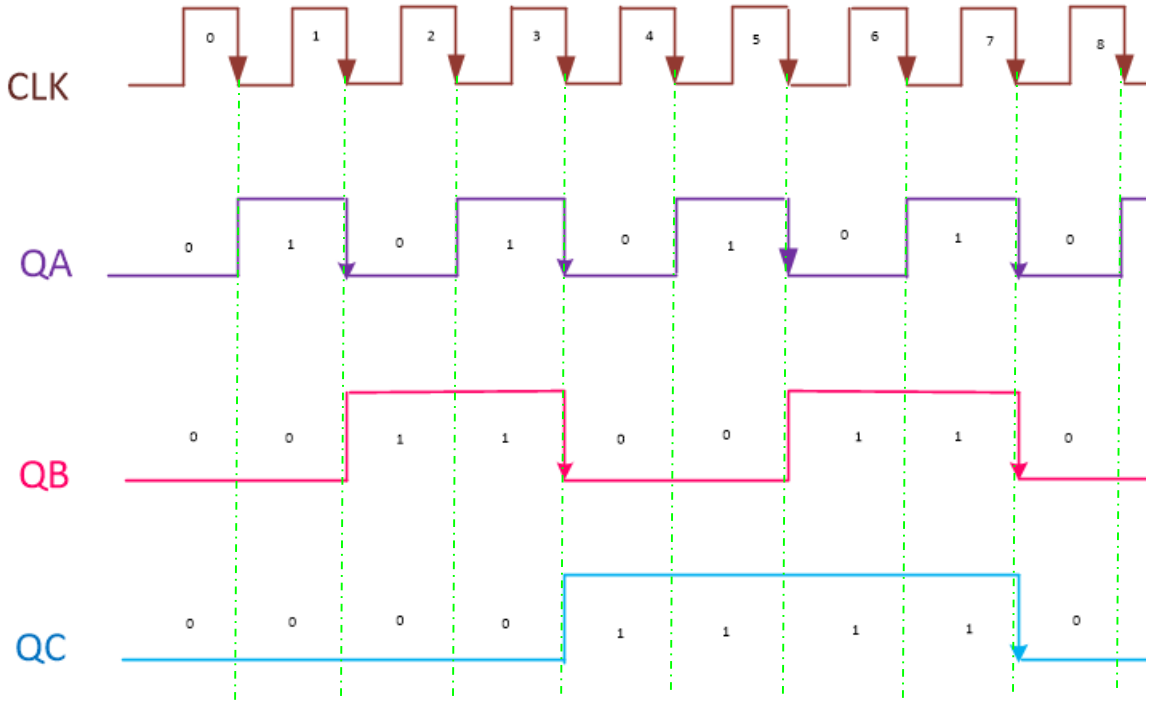
Serial counter with Preset/Clear input:



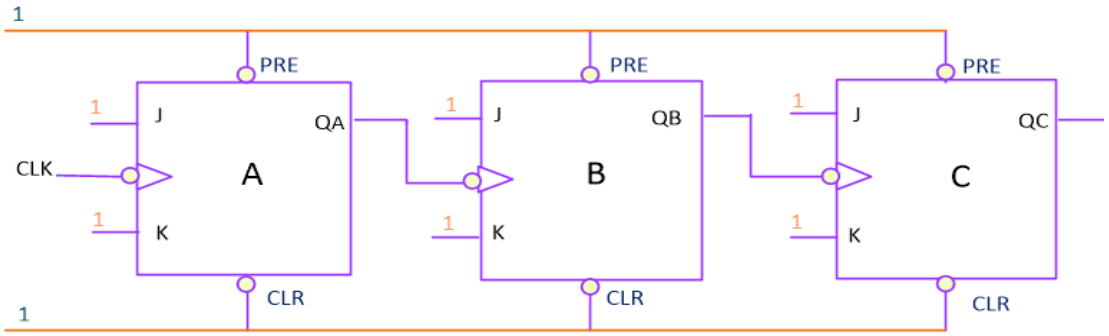


Mod 8 counter active high PRE & CLR





Mod 8 counter active low PRE & CLR

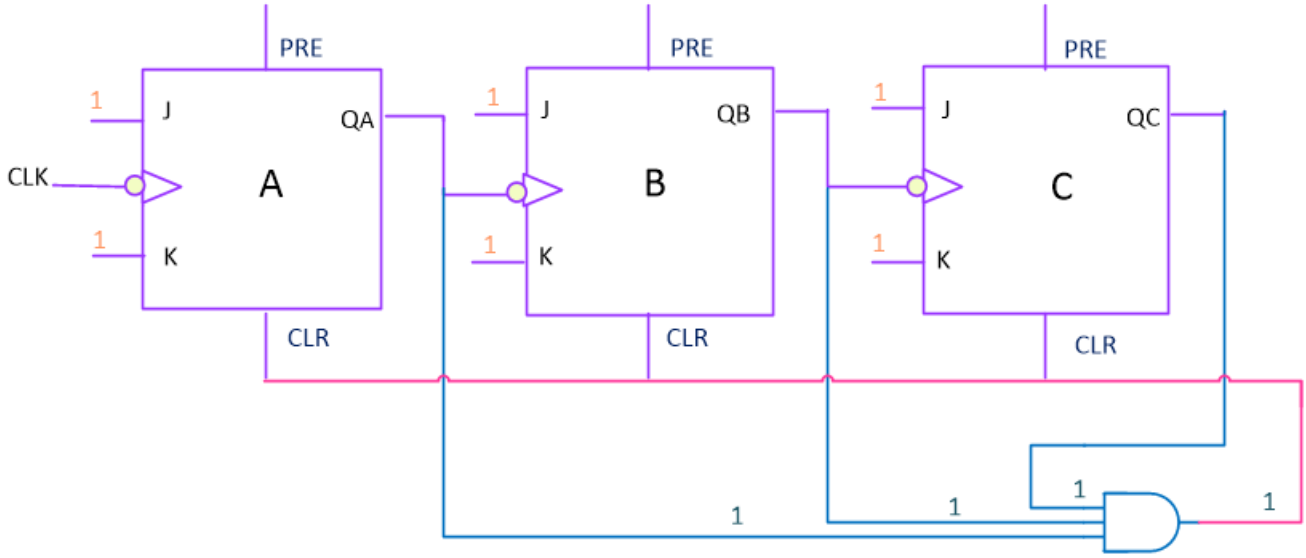


Mod 7 counter

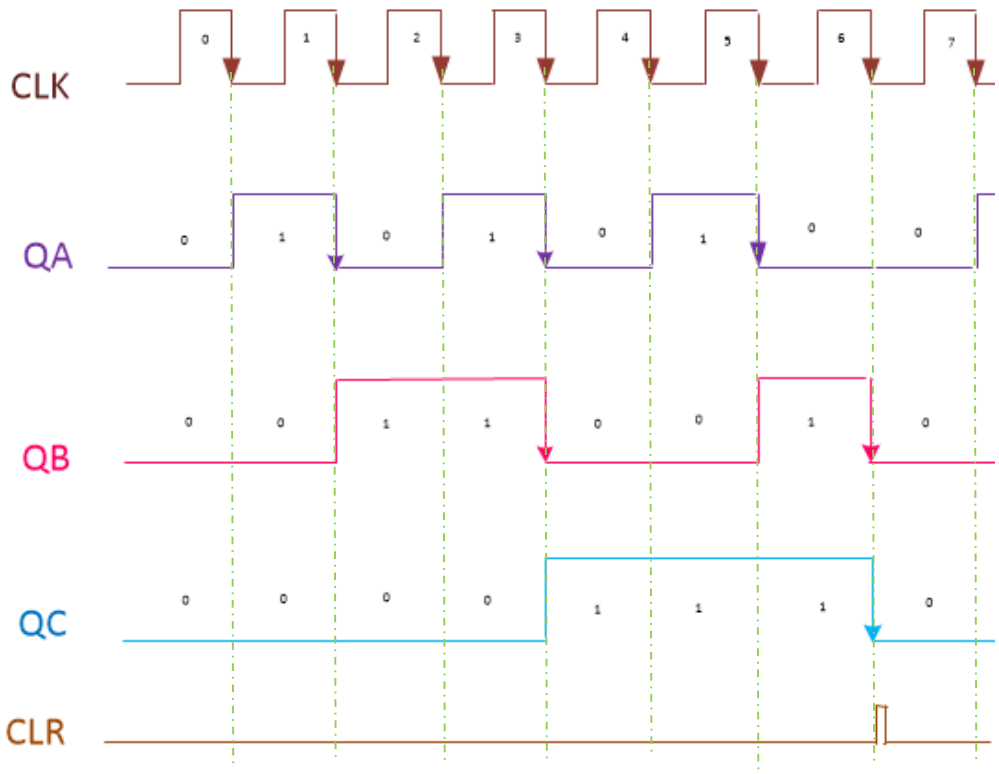
QCQBQA	Mod 8
0 0 0	0
0 0 1	1
0 1 0	2
0 1 1	3
1 0 0	4
1 0 1	5
1 1 0	6
1 1 1	7
0 0 0	8 recycle

Temporary state
Used to clear the counter

QCQBQA	Mod 7
0 0 0	0
0 0 1	1
0 1 0	2
0 1 1	3
1 0 0	4
1 0 1	5
1 1 0	6
0 0 0	7 recycle



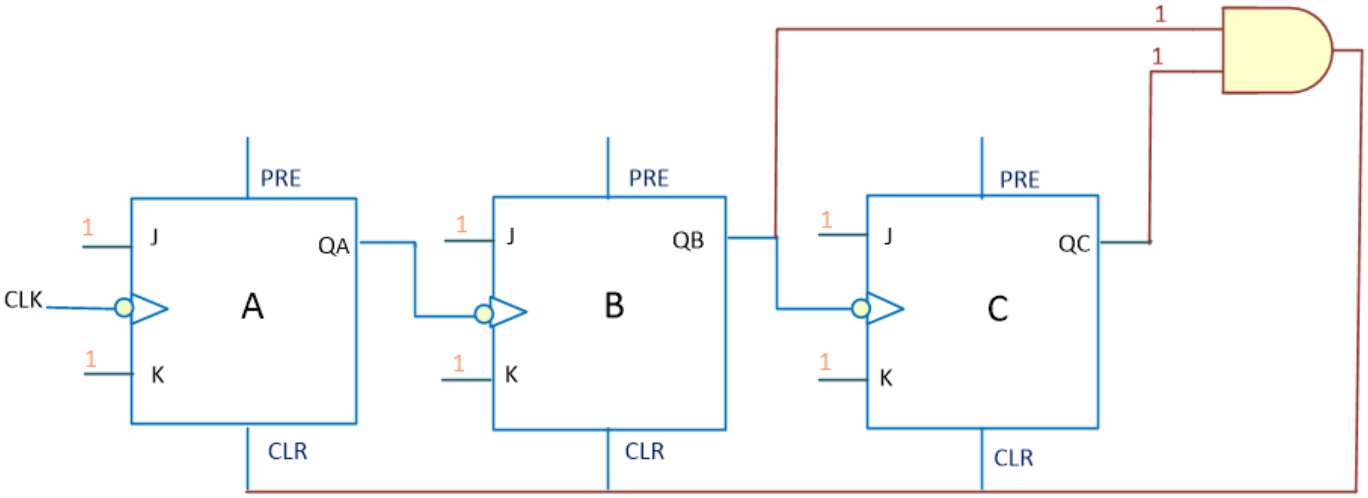
The counter would function normally until the 111 condition was reached at which point it would immediately reset to 000 state, ignoring the temporary execution of the 111 state the counter would go from 110 to 000 and then recycle back to 000 resulting in a mod 7 counter

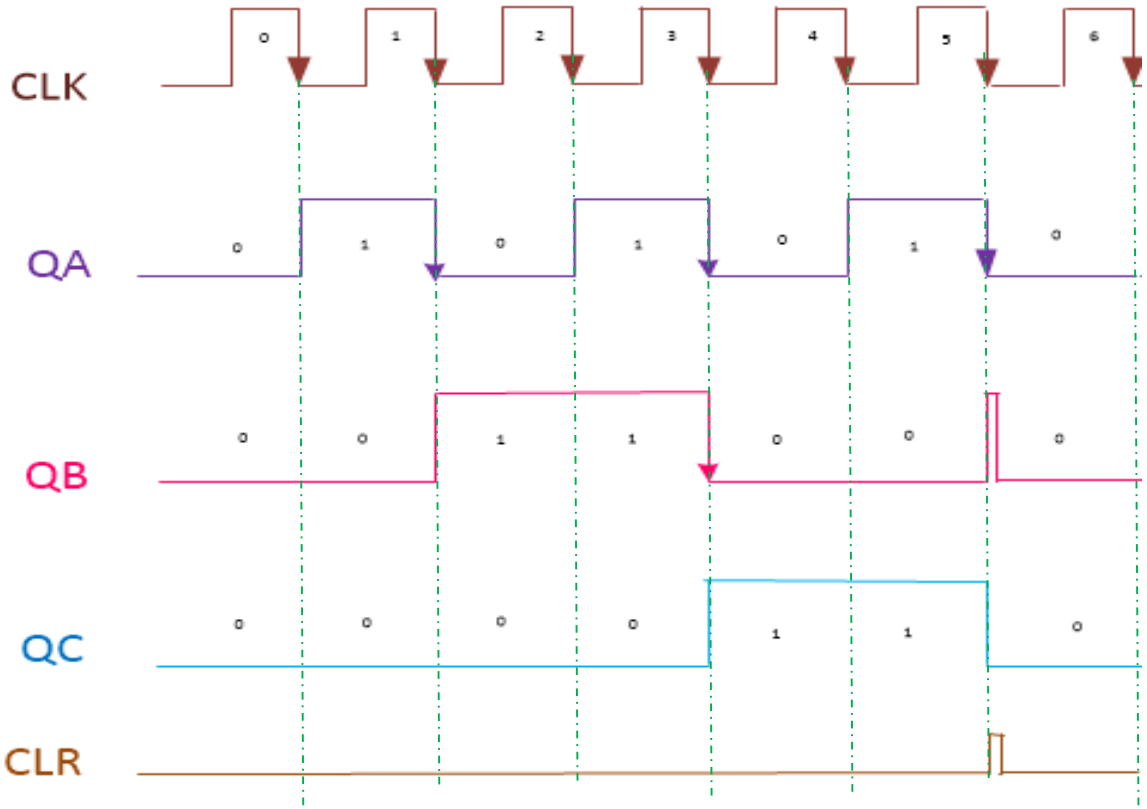


Mod 6 asynch. Counter

QCQBQA	Mod 6
0 0 0	0
0 0 1	1
0 1 0	2
0 1 1	3
1 0 0	4
1 0 1	5
1 1 0	
0 0 0	6 recycle

Used to clear the counter


1
1
PRE
PRE
PRE
1
J
QA
1
J
QB
1
J
QC
CLK
A
B
C
1
K
1
K
1
K
CLR
CLR
CLR

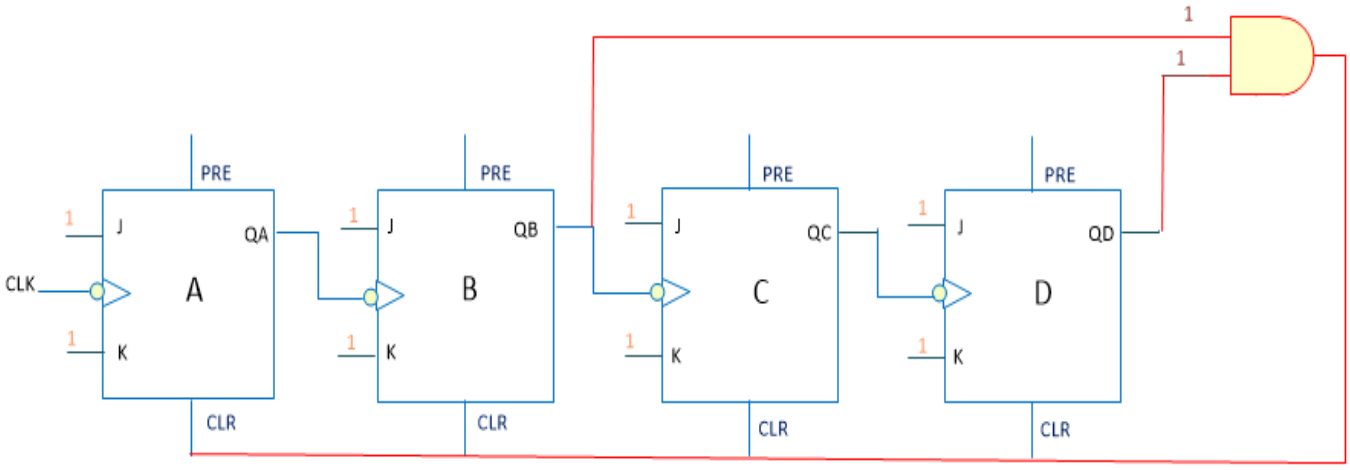

CLK
QA
QB
QC
CLR

ex: construct a mod 10 asynch. Counter that will count from 0000 to 1001 (BCD count)

QDQCQBQA	Mod 10
0 0 0 0	0
0 0 0 1	1
0 0 1 0	2
0 0 1 1	3
0 1 0 0	4
0 1 0 1	5
0 1 1 0	6
0 1 1 1	7
1 0 0 0	8
1 0 0 1	9
1 0 1 0	
0 0 0 0	10 recycle

Used to clear the counter

Note: this type of counter is called Decade counter



H.W:

Show how an asynch. Counter can be implemented having a modulus of 12 with a straight binary sequence from 0000 to 1011

ex: construct serial counter using PRE/CLR input flip flop that count in the following sequence

C B A	CLK	Y (cct.)
0 0 0	0	0
0 0 1	1	1
0 1 0	2	0
0 1 1	3	0
1 0 0	4	0
1 0 1	5	1
1 1 0	6	0
1 1 1	7	0
0 0 0	8	

skip

$$Y = A\bar{B}\bar{C} + A\bar{B}C = A\bar{B}\,(\bar{C} + C) = A\bar{B}$$