8086 Microprocessor and its Memory and Input / Output Interface

The 8086, announced in 1978, was the first 16-bit microprocessor introduced by Intel Corporation. The 8086 is manufactured using *high-performance metal-oxide semiconductor technology*, and the circuitry on its chips is equivalent to approximately 29000 transistors. It is housed in a 40-pin dual in-line package. As seen from Pin diagram of the 8086 (Figure 1) that many of its pins have multiple function.

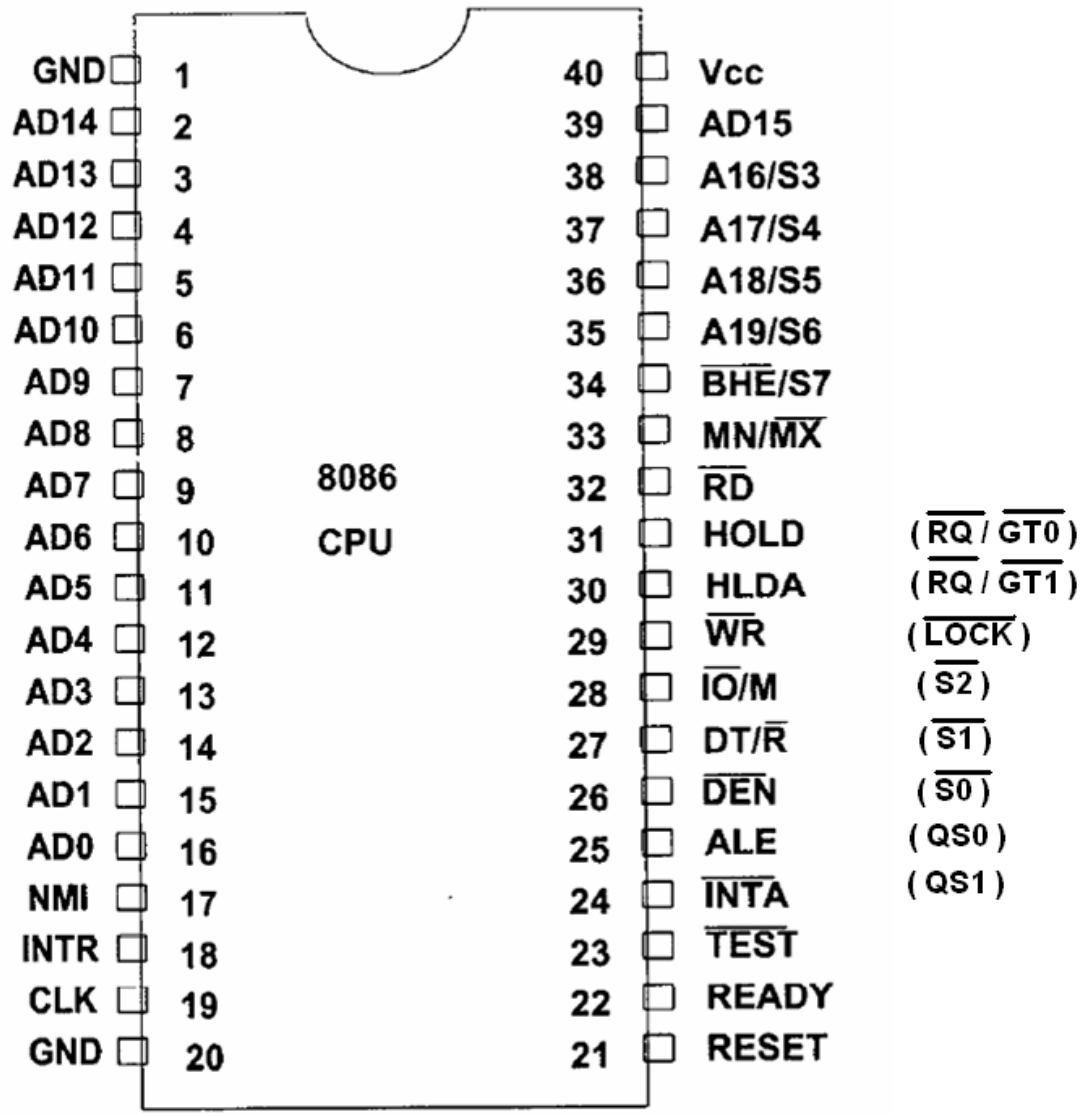

Fig-1- Pin diagram of the 8086

The 8086 can be configuring to work in either of two modes:

- The *minimum mode* is selected by applying logic 1 to the $MN/\overline{MX}$ input lead. Minimum mode 8086 systems are typically smaller and contain a single microprocessor.
- The *maximum mode* is selected by applying logic 0 to the $MN/\overline{MX}$ input lead. Maximum mode configures 8086 systems for use in larger systems and with multiple processors.

Depending on the mode of operation selected, the assignments for a number of pins on the microprocessor package are changed. As Figure 1 shows, the pin function of the 8086 specified in parentheses relate to a maximum-mode system.

Figure 2 below list the names, types and functions of the 8086 signals

Common signals		
Name	Function	Type
AD15-AD0	Address /data bus	Bidirectional
A19/S6-A16/S3	Address / status	Output
MN/$\overline{MX}$	Minimum/Maximum mode control	Input
$\overline{RD}$	Read control	Output
$\overline{TEST}$	Wait on test control	Input
READY	Wait state control	Input
RESET	System reset	Input
NMI	Non-maskable interrupt request	Input
INTR	Interrupt request	Input
CLK	System clock	Input
V_{CC}	+5 volt	Input
GND	Ground	Input

(a)

Minimum mode signals(MN/$\overline{MX}$=V_{CC})		
Name	Function	Type
HOLD	Hold request	Input
HLDA	Hold acknowledgment	Output
$\overline{WR}$	Write control	Output
M\$\overline{IO}$	IO/memory control	Output
DT\$\overline{R}$	Data transmit /receive	Output
$\overline{DEN}$	Data enable	Output
$\overline{BHE}$ \S7	Bank high enable/Status line 7	Output
ALE	Address latch enable	Output
$\overline{INTA}$	Interrupt acknowledgment	Output

(b)

Maximum mode signals(MN/$\overline{MX}$=Ground)		
Name	Function	Type
$\overline{RQ}$/GT1,0	Request/grant bus access control	Bidirectional
$\overline{LOCK}$	Bus priority lock control	Output
$\overline{S2} - \overline{S0}$	Bus cycle status	Output
QS1, QS0	Instruction queue status	Output

(c)

Figure 2 (a) signals common to both minimum and maximum mode.

(b) Unique minimum-mode signals. (c) Unique maximum-mode signals.

MINIMUM MODE INTERFACE SIGNALS

- **Address/Data Bus**

The address bus is 20 bits long and consists of signal lines A_0 (the LSB) to A_{19} (the MSB).The data bus is 16 bits long and consists of signals lines D_0 (the LSB) to D_{15} (the MSB).we see that address bus lines **A_0** through **A_{15}** and data bus lines **D_0** through **D_{15}** are multiplexed. For this reason, these leads are labeled **AD_0** through **AD_{15}**. By multiplexed we mean that the same physical pin carries an address bit at one time and the data bit at another time. When acting as a data bus, they carry read/write data for memory, input/output data for I/O devices, and interrupt-type codes from an interrupt controller.

- **Status signals**

The four most significant address lines, A_{19} through A_{16} are also multiplexed, but with status signals S_6 through S_3. These status bits are output on the bus at the same time that data are transferred over the other bus lines. Bits S_4 and S_3 together form a 2-bit binary code that identifies which of the internal segment registers was used to generate the physical address that was output on the address bus during the current bus cycle as shown in Figure 3. Status line S_5 reflects the status of logic level of the internal interrupt enable flag. Status line S_6 is always at the 0 logic level.

S_4	S_3	Address Status
0	0	**Extra** segment
0	1	**Stack** segment
1	0	**Code** segment
1	1	**Data** segment

Figure 3 address bus status codes

- **The control signals**

These are provided to support the memory and I/O interfaces of the 8086.

- **ALE** Address Latch Enable signal: when the pulse at logic 1 it indicates that the bits on AD15-AD0 are address bits, and when it at logic 0 it indicates that the bits on AD15-AD0 are data bits. This signal is used primarily to latch the address from the multiplexed bus and generate a separate address lines. This address can be latched in external circuitry on the 1-to-0 edge pulse at ALE.
- $\mathbf{M/\overline{IO}}$ Memory/IO signal: tells external circuitry whether a memory or I/O transfer is taking place over the bus. (Logic 1 for memory operation, logic 0 for I/O operation)
- $\mathbf{DT/\overline{R}}$ data transmit/receive signal: when this line is logic 1 the bus is in Transmit Mode (data are either written into memory or output to an I/O device). When this line is logic 0 the bus is in Receive Mode (data are either read from memory or input to an I/O device).
- $\mathbf{\overline{BHE}}$ bank high enable signal: logic 0 on this line is used as a memory enable signal for the most significant byte half of the data bus, D_8 through D_{15}.So the BHE is low for read, write, and interrupt acknowledge cycles when a byte is to be transferred on the high portion of the bus. This line also carries status bit S_7.The S7 status information is low for the first interrupt acknowledge cycle.
- $\mathbf{\overline{RD}}$ read signal: indicate that a read bus cycle is in progress.
- $\mathbf{\overline{WR}}$ write signal: indicate that a write bus cycle is in progress.
- $\mathbf{\overline{DEN}}$ data enable signal: during read operations, this signal is also supplied to enables external devices to supply data to the microprocessor.
- **READY signal**: used to insert wait states into the bus cycle so that it is extended by a number of clock periods.

- **Interrupt signals:** (INTR, $\overline{\text{INTA}}$, $\overline{\text{TEST}}$, NMI,RESET)

INTR is an input to the 8086 that can be used by an external device to signal that it needs to be serviced. Logic 1 at INTR represents an active interrupt request. When the MPU recognizes an interrupt request, it indicates this fact to external circuits with pulses to logic 0 at the $\overline{\text{INTA}}$ output.

The $\overline{\text{TEST}}$ input is also related to the external interrupt interface. For example, execution of a WAIT instruction causes the 8086 to check the logic level at the $\overline{\text{TEST}}$ input. If logic 1 is found at this input, the MPU suspends operation and goes into what is known as the idle state. The MPU no longer executes instructions; instead, it repeatedly checks the logic level of the input waiting for its transition back to logic 0. As $\overline{\text{TEST}}$ switches to 0, execution resumes with the next instruction in the program. This feature can be used to synchronize the operation of the MPU to an event in external hardware.

There are two more inputs in the interrupt interface: nonmaskable interrupt (NMI) and reset (RESET). On the 0 — to —1 transition of NMI, control is passed to a nonmaskable interrupt service routine at completion of execution of the current instruction. NMI is the interrupt request with highest priority and cannot be masked by software.

The RESET input is used to provide a hardware reset for the MPU. Switching RESET to logic 0 initializes the internal registers of the MPU and initiates a reset service routine.

- **Direct memory access (DMA) interface signals:** (HOLD, $\overline{\text{HOLA}}$)

The DMA interface of 8086 minimum-mode microcomputer system consists of the HOLD and $\overline{\text{HOLA}}$ signals, When an external device wants to take control of the system bus, it signals this fact to the MPU by switching HOLD to the logic 1. For

example, when the HOLD input of the 8086 becomes active, it enters the hold state at the completion of the current bus cycle. When in the hold state, signal lines are all put in the high-z state (high impedance). The 8086 signals external devices that it is in this state by switching its HLDA output to the logic 1level.

- $\mathbf{MN/\overline{MX}}$ minimum mode / maximum mode line: when is at logic 1 minimum mode is selected, otherwise, connecting it to logic 0 the maximum mode is select. Figure -4- shown block diagram of the 8086 minimum –mode

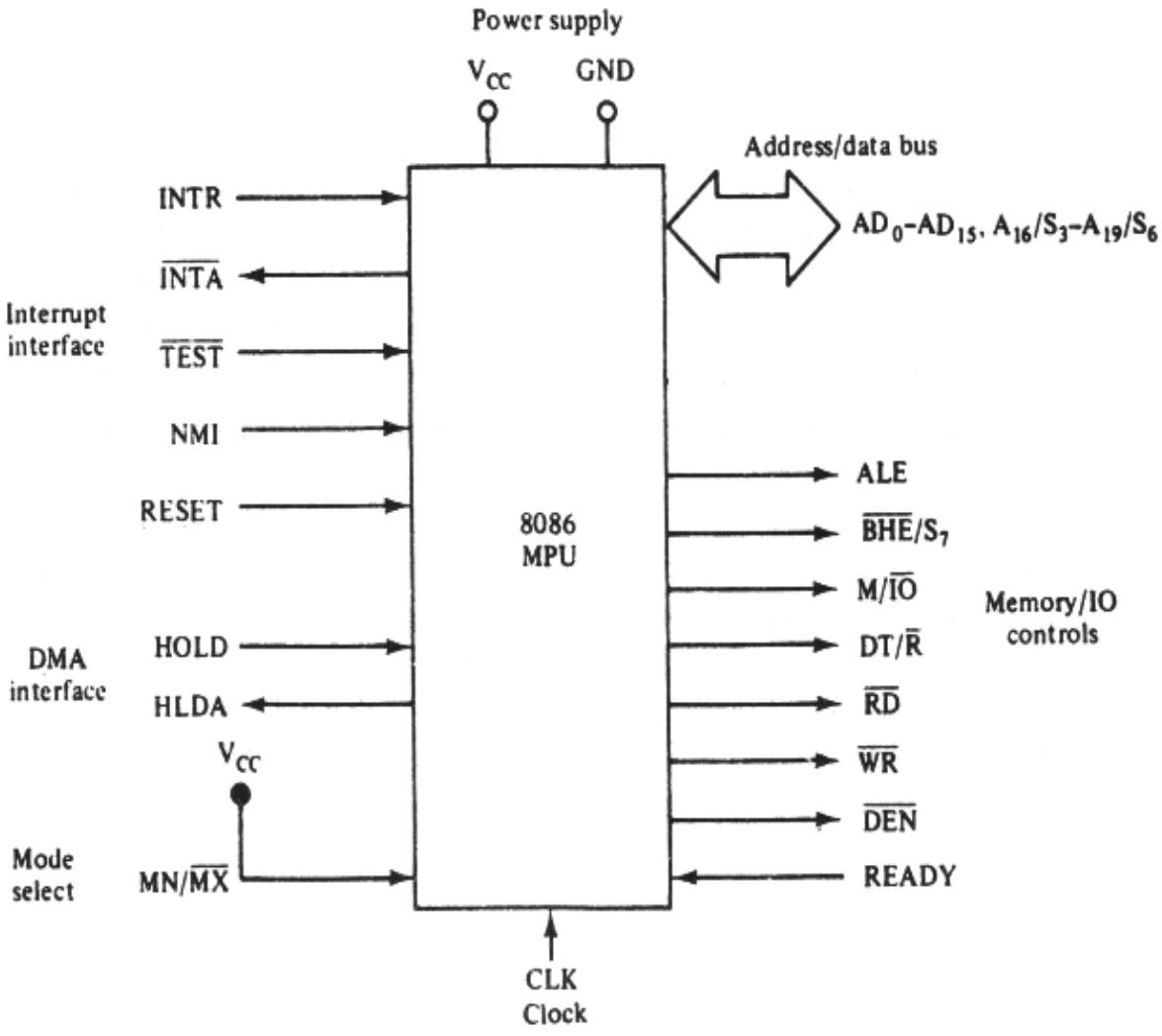

Figure 4 shown block diagram of the 8086 minimum –mode

MAXIMUM MODE INTERFACE SIGNALS

When the 8086 microprocessor is set for the maximum-mode configuration, it produces signals for implementing a *multiprocessor system environment*. By *multiprocessor system environment* we mean that multiple microprocessors exist in the system and that each processor executes its own program.

8288 bus controller: Bus Commands and Control Signals

During the maximum mode (as shown in figure 6) operation, the $\overline{WR}$, $M/\overline{IO}$, $DT/\overline{R}$, $\overline{DEN}$, ALE and $\overline{INTA}$ signals are no longer produced by the 8086. Instead, it outputs a status code on three signals lines, $\overline{S_0}$, $\overline{S_1}$, and $\overline{S_2}$ prior to the initiation of each bus cycle.

Status inputs			CPU Cycle	8288 Command	Meaning
$\overline{S2}$	$\overline{S1}$	$\overline{S0}$			
0	0	0	Interrupt Acknowledge	$\overline{INTA}$	Interrupt acknowledge
0	0	1	Read I/O port	$\overline{IORC}$	I/O read control
0	1	0	Write I/O port	$\overline{IOWC}$, $\overline{AIOWC}$	I/O write control, Advanced I/O write control
0	1	1	Halt	None	---
1	0	0	Instruction Fetch	$\overline{MRDC}$	Memory read control
1	0	1	Read Memory	$\overline{MRDC}$	Memory read control
1	1	0	Write Memory	$\overline{MWTC}$, $\overline{AMWC}$	Memory write control, advanced memory write control
1	1	1	Passive	None	---

Figure-5 Bus status codes

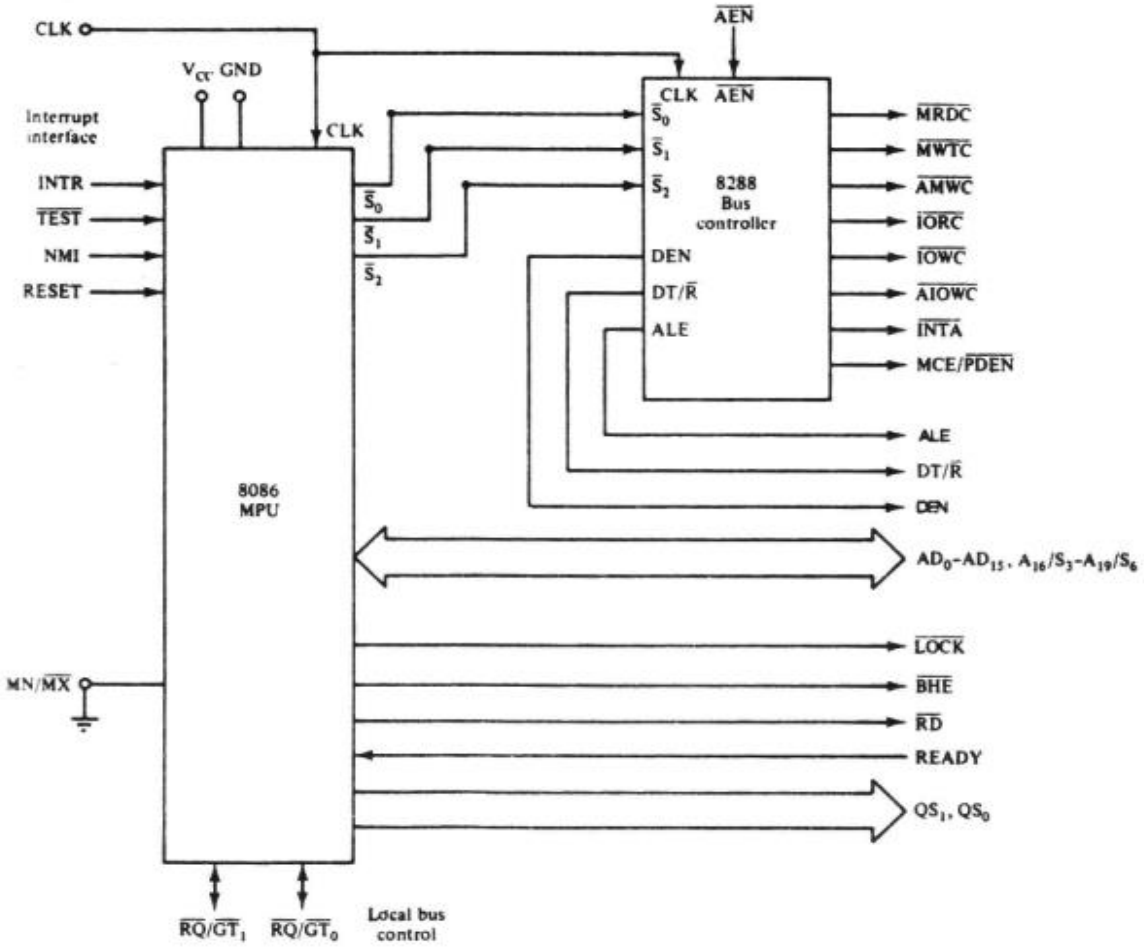

Figure-6 maximum – mode block diagram with the 8288 bus controller

- $\overline{S_0}, \overline{S_1}, \overline{S_2}$ bus status code : These three bit identifies which type of bus cycle is to follow, these bits are input to the external *bus controller* device, the **8288**, which decodes them to identify the type of MPU bus cycle, as shown in figure 5. In addition the other control signal produced by the 8288 *bus controller* consist of DEN, $DT/\overline{R}$, and ALE. These three signals provide the same functions as those described for the minimum mode.

$\overline{LOCK}$ signal: this signal is meant to be output (logic 0) whenever the processor wants to lock out the other processors from using the bus.

- **Queue Status code Signals** (QS1, QS0): these two bits tell the external circuitry what type of information was removed from the queue. Figure-7 shows the four different queue status codes.

QS1	QS0	Queue Status
0 (low)	0	No Operation. During the last clock cycle, nothing was taken from the queue.
0	1	First Byte. The byte taken from the queue was the first byte of the instruction.
1 (high)	0	Queue Empty. The queue has been reinitialized as a result of the execution of a transfer instruction.
1	1	Subsequent Byte. The byte taken from the queue was a subsequent byte of the instruction.

Figure-7

Note that QS1QS0=01 indicates that the first byte of an instruction was taken off queue. As shown, the fetch of the next byte of the instruction is identified by the code 11.whenever the queue is reset due to a transfer of control, the reinitialization code 10 is output.

$\overline{\mathbf{RQ/GT1}}$, $\overline{\mathbf{RQ/GT0}}$: In a maximum-mode configuration, the minimum-mode HOLD and $\overline{\mathrm{HOLA}}$ interface of the 8086 is also changed. These two signals are replaced by request/grant lines $\overline{\mathrm{RQ/GT0}}$ and $\overline{\mathrm{RQ/GT1}}$. These two signals provide a prioritized bus access mechanism for accessing the local bus.

System Clock

The time base for synchronization of the internal and external operations of the microprocessor in a microcomputer system is provided by the *clock* (CLK) input signal. The *8284 clock generator* connects to the 8086 . (Figure -8)

The 8086 microprocessor is manufactured in three speeds: the **5-MHz** 8086, the **8-MHz** 8086-2 and the **10-MHz** 8086-1.

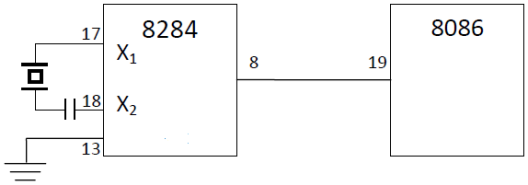

Figure -8 connecting the 8284 to the 8086