MEMORY CONTROL SIGNAL

Earlier we saw that similar control signals are produced in the maximum and minimum mode. Moreover, we found that in the minimum mode, the 8086 microprocessors produce all the control signals. But in the maximum mode, the 8288 bus controller produces them. Here we will look more closely at each of these signals and their functions with respect to memory interface operation.

Minimum-Mode Memory Control Signals

In the 8086 microcomputer system shown in Fig. -1-, which is configured for the minimum mode of operation, we find that the control signals provided to support the interface to the memory subsystem are **ALE, $\mathbf{M/\overline{IO}}$, $\mathbf{DT/\overline{R}}$, $\mathbf{\overline{RD}}$, $\mathbf{\overline{WR}}$,$\mathbf{\overline{DEN}}$** and $\mathbf{\overline{BHE}}$ These control signals are required to tell the memory subsystem when the bus is carrying a valid address, in which direction data are to be transferred over the bus, when valid write data are on the bus, and when to put read data on the bus. For example,

address latch enable (ALE) signals external circuitry that a valid address is on the bus. It is a pulse to the 1 logic level and is used to latch the address in external circuitry.

The memory / input-output ($M/\overline{IO}$) and data transmit/receive $DT/\overline{R}$ lines signal external circuitry whether a memory or I/O bus cycle is in progress and whether the 8086 will transmit or receive data over the bus.

During all memory bus cycles, $M/\overline{IO}$ is held at the 1 logic level. The 8086 switches $DT/\overline{R}$ to logic 1 during the data transfer part of the bus cycle, the bus in the transmit mode, and data are written into memory. On the other hand, it sets $DT/\overline{R}$ to logic 0 to signal that the bus is in the receive mode, which corresponds to reading of memory.

The signals read ($\overline{RD}$) and write ($\overline{WR}$) identify that a read or write bus cycle, respectively, is in progress. The 8086 switches $\overline{WR}$ to logic 0 to signal memory that a write cycle is taking place over the bus. On the other hand, $\overline{RD}$ is switched to logic 0 whenever a read cycle is in progress.

During all memory operations, the 8086 produces one other control signal, data enable ($\overline{DEN}$). Logic 0 at this output is used to enable the data bus.

bank high enable ($\overline{BHE}$) is used as a select input for the high bank of memory in the 8086`s memory subsystem. That is, logic 0 is output on this line during the address part of all the bus cycles in which data in the high-bank part of memory is to be accessed.

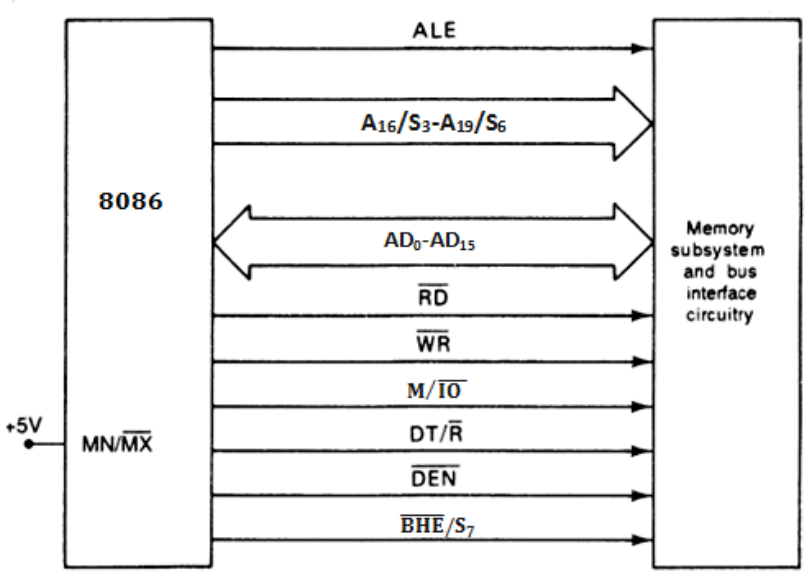


Fig-1-

Maximum-Mode Memory Control Signals

When the 8086 is configured to work in the maximum mode, it does not directly provide all the control signals to support the memory interface. Instead, an external bus controller, the 8288, provides memory commands and control signals. Figure-2- shows an 8086 connected in this way.

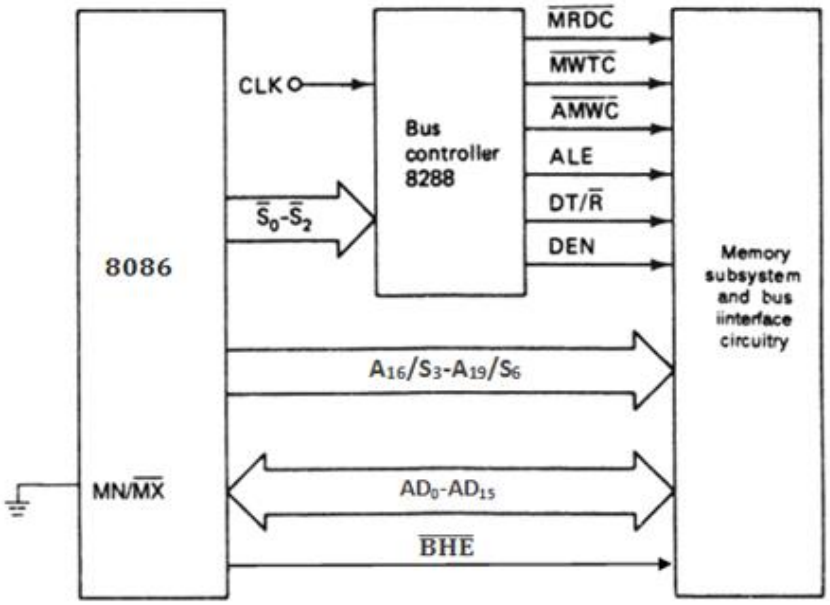


Fig-2-

Specifically, the ALE, $M/\overline{IO}$, $DT/\overline{R}$, $\overline{WR}$, $\overline{DEN}$ signal lines on the 8086 are changed. They are replaced with multiprocessor lock ($\overline{LOCK}$) signal, a bus status code ($\overline{S_2}$ $\overline{S_1}$ $\overline{S_0}$), and a queue status code (QS_1QS_0). The 8086 still does produce the signal $\overline{RD}$, which provides the same function as it did in minimum mode.

The 3-bit bus status code $\overline{S_2}$ $\overline{S_1}$ $\overline{S_0}$ is output prior to the initiation of each bus cycle. It identities which type of bus cycle is to follow. This code is input to the 8288 bus controller. Here it is decoded to identify which type of bus cycle command signals must be generated.

Figure-3- shows the relationship between the bus status codes and the types of bus cycles produced. Also shown in this chart are the names of the corresponding command signals that are generated at the outputs of the 8288.

Status Inputs			CPU Cycle	8288 Command
$\overline{S_2}$	$\overline{S_1}$	$\overline{S_0}$		
0	0	0	Interrupt acknowledge	$\overline{INTA}$
0	0	1	Read I/O port	$\overline{IORC}$
0	1	0	Write I/O port	$\overline{IOWC}$, $\overline{AIOWC}$
0	1	1	Halt	None
1	0	0	Instruction fetch	$\overline{MRDC}$
1	0	1	Read memory	$\overline{MRDC}$
1	1	0	Write memory	$\overline{MWTC}$, $\overline{AMWC}$
1	1	1	Passive	None

Fig-3-

For instance, the input code $\overline{S_2}\ \overline{S_1}\ \overline{S_0}$ equal to 100 indicates that an instruction fetch bus cycle is to take place. Since the instruction fetch is a memory read, the 8288 makes the memory read command ($\overline{MRDC}$) output switch to logic 0.

Another bus command provided for the memory subsystem is $\overline{S_2}\ \overline{S_1}\ \overline{S_0}$ equal to 110 This represents a memory write cycle and it causes both the memory write command ($\overline{MWTC}$) and advanced memory write command ($\overline{AMWC}$) outputs to switch to the 0 logic level.

The other control outputs produced by the 8288 are DEN, $\mathrm{DT}/\overline{\mathrm{R}}$, and ALE. These signals provide the same functions as those produced by the corresponding pins on the 8086 in the minimum system mode.

The two status signals, QS_0 and QS_1, form an instruction queue code. This code tells the external circuitry what type of information was removed from the queue during the previous clock cycle. The four different queue statuses, QS_0QS_1= 01 indicates that the first byte of an instruction was taken from the queue. The next byte of the instruction that is fetched is identified by queue status code 11. Whenever the queue is reset (e.g., due to a transfer of control) the reinitialization code 10 is output. Similarly, if no queue operation occurred, status code 00 is output.

The bus priority lock ($\overline{LOCK}$) signal, can be used as an input to a bus arbiter. The bus arbiter is used to lock other processors off the system bus during accesses of common system resources such as global memory in a multiprocessor system. The READY signal is used to interface slow memory devices.

The $\overline{\mathrm{BHE}}$ performs the same function as it did in the minimum-mode system. That is, it is used as an enable input to the high bank of memory.

READ AND WRITE BUS CYCLES

we introduced the status and control signals associated with the memory interface. Here we studying the sequence in which they occur during the read and write bus cycles of memory.

- **Read Cycle**

Figure -4-(a) shows the memory interface signals of a minimum-mode 8086 system. Here their occurrence is illustrated relative to the four time states T1, T2, T3, and T4 of the 8086's bus cycle. Let us trace the events that occur as data or instructions are read from memory.

The read bus cycle begins with state T1. During this period, the 8086 outputs the 20-bit address of the memory location to be accessed on its multiplexed address/data bus AD_0 through AD_{15} and multiplexed lines A_{16}/S_3 through A_{19}/S_6. Note that at the same time a pulse is also produced at ALE. The high level of this pulse should be used to latch the address in external circuitry.

Also we see that at the start of T1, signals $M/\overline{IO}$ is set to logic 1 and $DT/\overline{R}$ is set to the 0 logic level. This indicates to circuitry in the memory subsystem that a memory cycle is in progress and that the 8086 is going to receive data from the bus.

Note that these signals are maintained at these logic levels throughout all four periods of the bus cycle.

Beginning with state T2, status bits S_3 through S_6 are output on the upper four address bus lines A_{16} through A_{19}. Remember that bits S_3 and S_4 identify to external circuitry which segment register was used to generate the address just output. This status information is maintained through periods T3 and T4. $\overline{BHE}$ is output along with the address during T1.

The address/data bus lines AD_0 through AD_{15} are put in the high—Z state during T2.

Late in period T2, $\overline{RD}$ is switched to logic 0. This indicates to the memory subsystem that a read cycle is in progress. $\overline{DEN}$ is switched to logic 0 to enable external circuitry to allow the data to move from memory onto the microprocessor's data bus. As shown in the waveforms, input data are read by the 8086 during T3.

The memory must provide valid data during T3 and maintain it until after the processor terminates the read operation. As shows, it is in T4 that the 8086 switches $\overline{RD}$ to the inactive 1 logic level to terminate the read operation. $\overline{DEN}$ returns to its inactive logic level during T4 to disable the external circuitry, which allows data to move from memory to the processor. The read cycle is now complete.

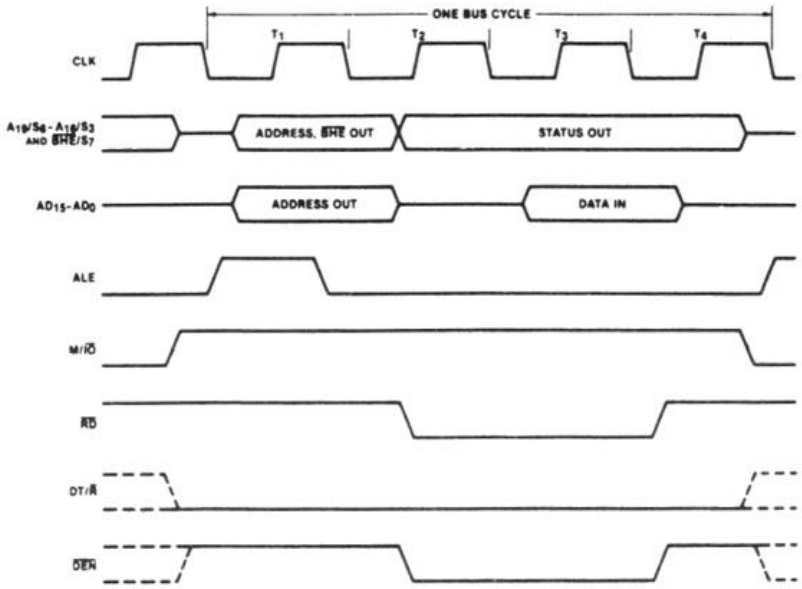


Fig-4-(a)

Figure -4-(b) shows a read cycle of 8-bit data in a maximum-mode 8086-based microcomputer system. These waveforms are similar to those given for the minimum-mode read cycle in Fig. -4-(a). Comparing these two timing diagrams, we see that the address and data transfers that take place are identical. In fact, the only difference found in the maximum-mode waveforms is that a bus cycle status code, $\overline{S_2}\ \overline{S_1}\ \overline{S_0}$, is output just prior to the beginning of the bus cycle. This status information is decoded by the 8288 to produce control signals ALE, $\overline{MRDC}$, $\mathrm{DT}/\overline{\mathrm{R}}$ and DEN.

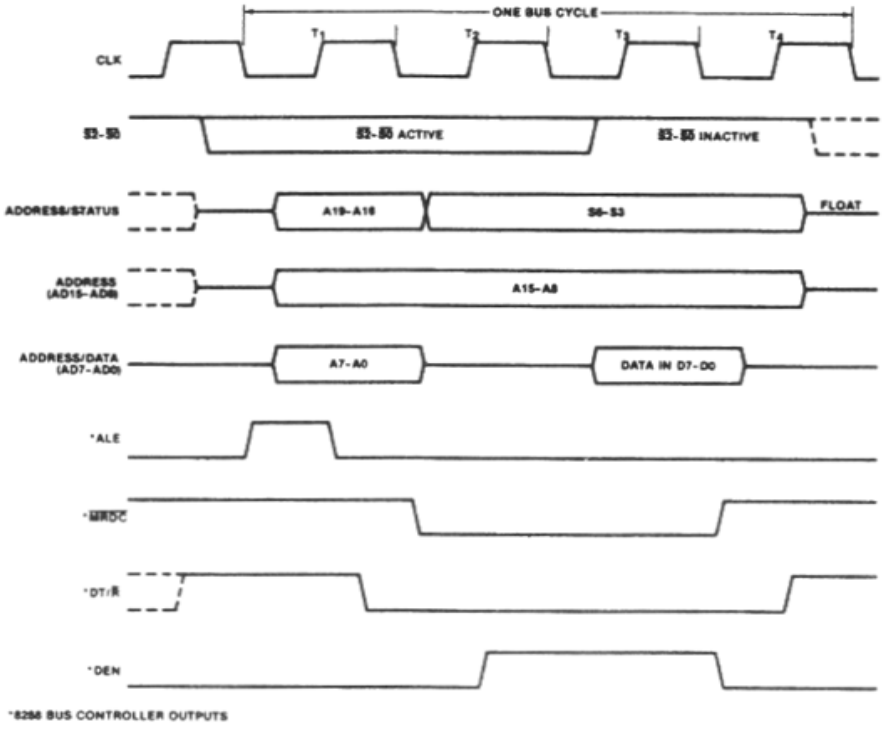


Fig-4-(b)

- **Write cycle**

The write bus cycle is similar to that given for a read cycle. For the minimum mode write cycle waveforms, we find that during T1, the address is output and latched with the ALE pulse. This is identical to the read cycle, $\overline{\mathrm{BHE}}$ is output along with the address. Moreover, $\mathrm{M}/\overline{\mathrm{IO}}$ is set to logic 1 to indicate that a memory cycle is in progress , this time $\mathrm{DT}/\overline{\mathrm{R}}$ is switched to logic 1. This signals external circuits that the 8086 is going to transmit data over the bus.

As T2 starts, the 8086 switches $\overline{\mathrm{WR}}$ to logic 0. This tells the memory subsystem that a write operation is to follow over the bus. The 8086 puts the data on the bus late in T2 and maintains the data valid through T4. The writing of data into memory starts as $\overline{\mathrm{WR}}$ becomes 0, and continues as it changes to 1 early in T4. $\overline{\mathrm{DEN}}$ enables the external circuitry to provide a path for data from the processor to the memory. This completes the write cycle.

Figure-5- illustrates the write bus cycle timing of the 8086 in maximum mode.

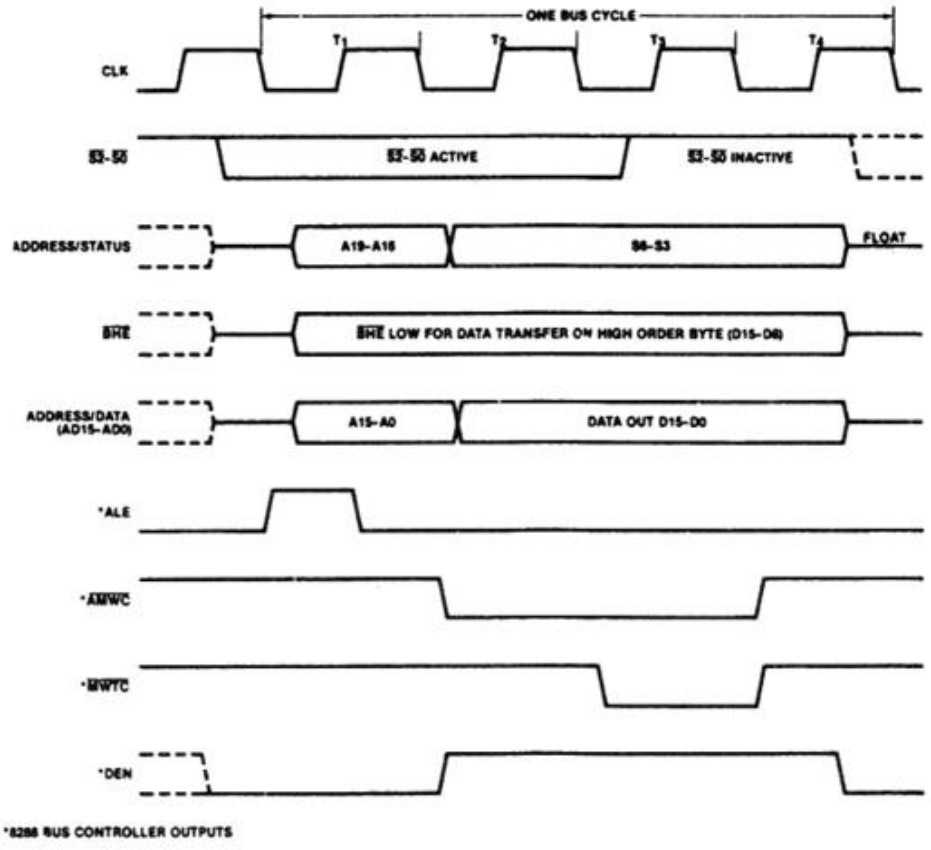


Fig-5-

MEMORY INTERFACE CIRCUITS

We describes the memory interface circuits of an 8086-based microcomputer system. Figure-6- shows a memory interface diagram for a maximum-mode 8086-based microcomputer system.

Here we find that the interface includes the

- 8288 bus controller
- address bus latches and an address decoder
- data bus transceiver/buffers
- bank read and write control logic.

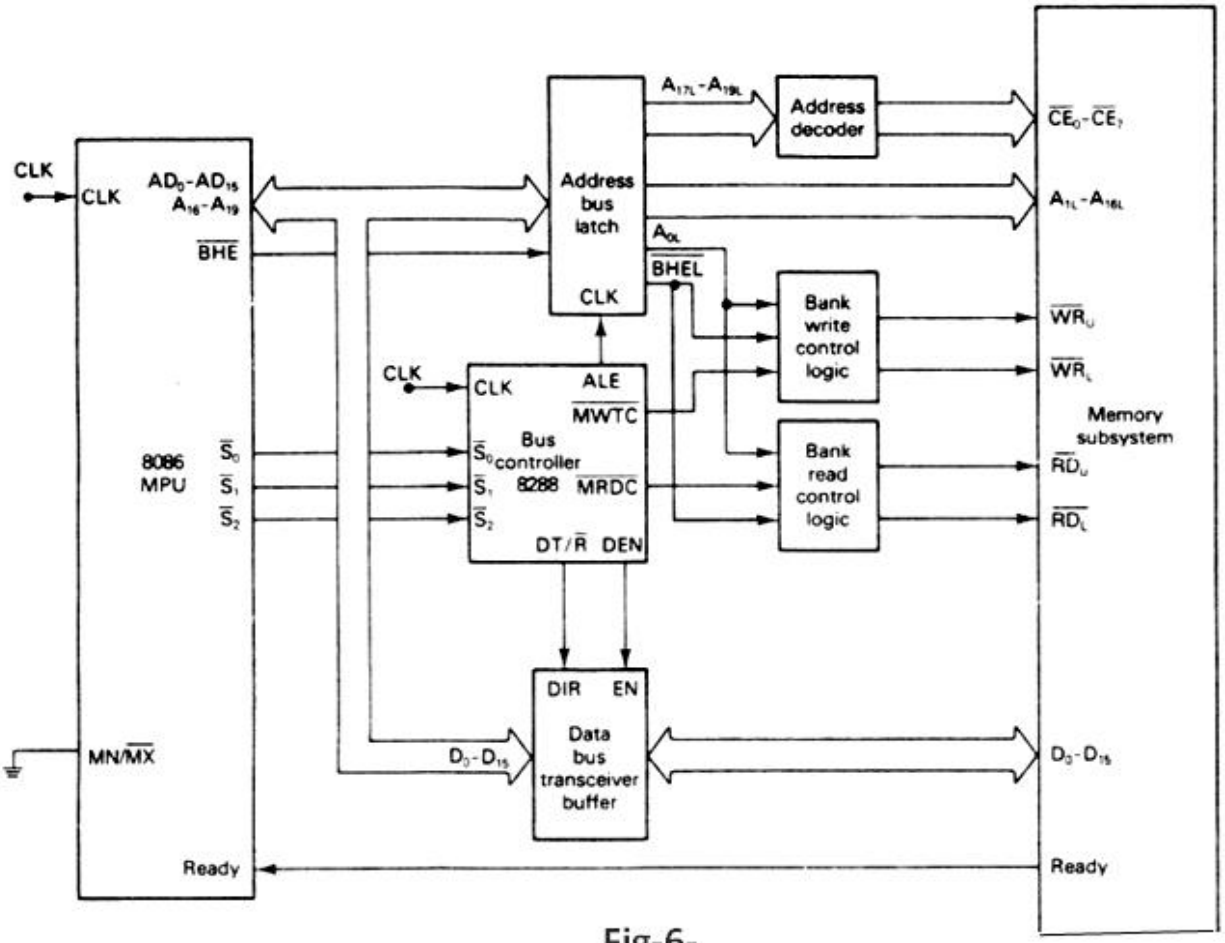


Fig-6-

Looking at Fig.-6-, we see that bus status code signals $\overline{S_2}$ $\overline{S_1}$ $\overline{S_0}$ which are outputs of the 8086, are supplied directly to the 8288 bus controller. Here they are decoded to produce the command and control signals needed to coordinate data transfers over the bus.

For example, the code $\overline{S_2}$ $\overline{S_1}$ $\overline{S_0}$ = 101 indicates that a data memory read bus cycle is in progress. This code makes the $\overline{MRDC}$ command output of the bus control logic switch to logic 0. Note in Fig.-6- that $\overline{MRDC}$ is applied to the bank read control logic.

Next let us look at how the address bus is latched, buffered. and decoded. Looking

at Fig.-6-, we see that address lines A_0 through A_{19} are latched along with control signal $\overline{\text{BHE}}$ in the address bus latch. The latched address lines A_{17L} through A_{19L} are decoded to produce chip enable outputs $\overline{CE_0}$ through $\overline{CE_7}$.

Notice that the 8288 bus controller produces the address latch enable (ALE) control signal from $\overline{S_2}$ $\overline{S_1}$ $\overline{S_0}$. ALE is applied to the CLK input of the latches and strobes the bits of the address and bank high enable $\overline{\text{BHE}}$ signal into the address bus latches.

Latched address lines A_{1L} through A_{16L} and $\overline{CE_0}$ through $\overline{CE_7}$ are applied directly to the memory subsystem.

During read bus cycles, the $\overline{MRDC}$ output of the bus control logic enables the bytes of data at the outputs of the memory subsystem onto data bus lines D_0 through D_{15}.

During read operations from memory, the bank read control logic determines whether the data are read from one of the two memory banks or from both. This depends on whether a byte- or word-data transfer is taking place over the bus.

Similarly during write bus cycles, the $\overline{MWTC}$ output of the bus control logic enables bytes of data from the data bus D_0 through D_{15} to be written into the memory. The bank write control logic determines to which memory bank the data are written.

Note in Fig.-6- that in the bank write control logic the latched bank high enable signal $\overline{\mathrm{BHEL}}$ and address line A_{0L} are gated with the memory write command signal $\overline{MWTC}$ to produce a separate write enable signal for each bank. These signals are denoted as $\overline{WR_U}$, and $\overline{WR_L}$, For example, if a word of data is to be written to memory over data bus lines D_0 through D15, both $\overline{WR_U}$ and $\overline{WR_L}$ are switched to their active 0 logic level.

Similarly the memory read control logic uses $\overline{MRDC}$, A_{0L}, and $\overline{\mathrm{BHEL}}$ to generate $\overline{RD_U}$ and $\overline{RD_L}$ signals for bank read control.

The bus transceivers control the direction of data transfer between the MPU and memory subsystem. In Fig.-6-, we see that the operation of the transceivers is controlled by the $\mathrm{DT}/\overline{\mathrm{R}}$ and DEN outputs of the bus controller.

DEN is applied to the EN input of the transceivers and enables them for operation. This happens during all read and write bus cycles. $\mathrm{DT}/\overline{\mathrm{R}}$ selects the direction of data transfer through the devices. Note that it is supplied to the DIR input of the data bus transceivers. When a read cycle is in progress, $\mathrm{DT}/\overline{\mathrm{R}}$ is set to 0 and data are passed from the memory subsystem to the MPU. On the other hand, when a write cycle is taking place, $\mathrm{DT}/\overline{\mathrm{R}}$ is switched to logic 1 and data are carried from the MPU to the memory subsystem.

For the minimum mode, the memory interface is similar to figure-6-except that

- The signals *ALE*, $\overline{\mathrm{DEN}}$ and $\mathrm{DT}/\overline{\mathrm{R}}$ are deliver by 8086 directly.
- $\overline{MWTC}$ and $\overline{MRDC}$ are produced as shown in figure -7-.

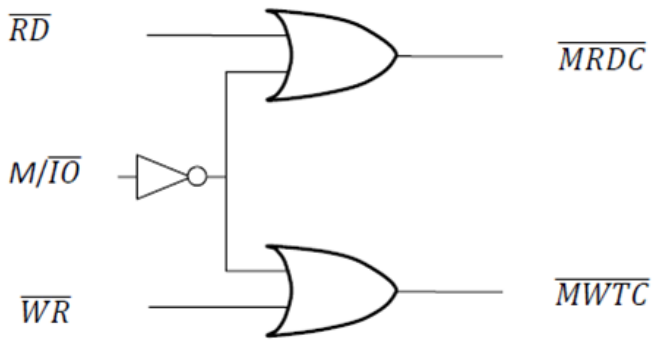
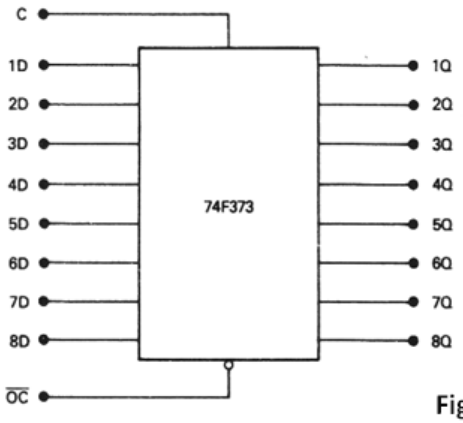


Fig-7-

Address Bus Latches and Buffers

The 74F373 (74LS373) is an example of an octal latch device that can be used to implement the address latch section of the 8086's memory interface circuit. A block diagram of this device is shown in Fig.-8-



Inputs			Output
$\overline{OC}$	Enable C	D	Q
L	H	H	H
L	H	L	L
L	L	X	Q_0
H	X	X	Z

Fig-8-

In the 8086 microcomputer system, the 20 address lines (AD_0 - AD_{I5} , A_{16} - A_{I9}) and the bank high enable signal $\overline{BHEL}$ are normally latched in the address bus latch. The circuit configuration shown in Fig.-9- can be used to latch these signals.

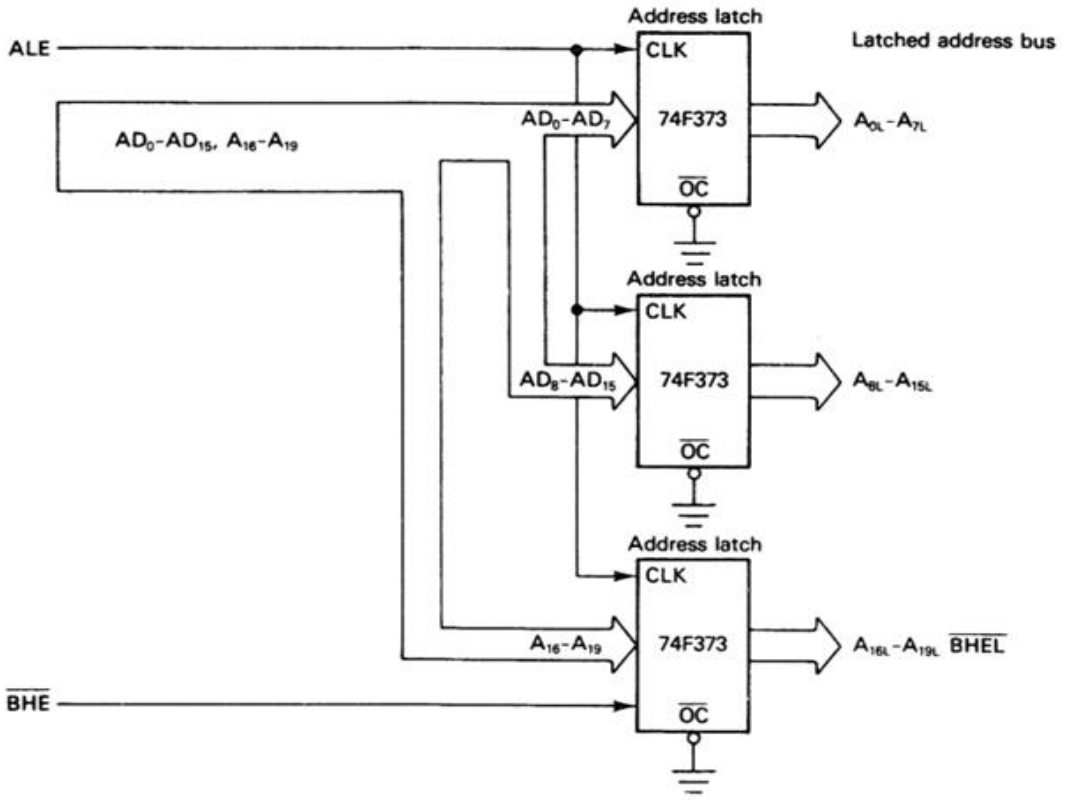


Fig-9-

Fixing $\overline{OC}$ at the 0 logic level permanently enables latched outputs A_{0L} through A_{19L} and $\overline{BHEL}$. Moreover, the address information is latched at the outputs as the ALE signal from the bus controller returns to logic 0 that is, when the CLK input of all devices is switched to logic 0.

Bank Write and Bank Read Control Logic

The memory of the 8086 microcomputer is organized in upper and lower banks. It requires separate write and read control signals for the two banks. The logic circuit Fig.-10- (a) shows how the bank write control signals, $\overline{WR_U}$ for the upper bank and $\overline{WR_L}$ for the lower bank can be generated from the bus controller signals $\overline{MWTC}$, the address bus latch signals A_{0L} and $\overline{BHEL}$. Two OR gates are used for this purpose.

Similar to the bank write control logic circuit, the bank read control logic circuit can be designed to generate $\overline{RD_U}$, the read for the upper bank of memory, and $\overline{RD_L}$, the read for the lower bank. Figure-10-(b) illustrates such a circuit. Note that the circuit uses the $\overline{MRDC}$ signal from the bus controller.

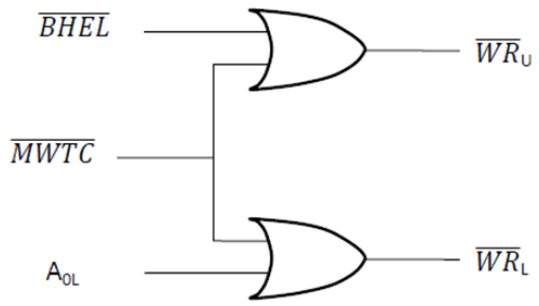


Fig-10- (a)

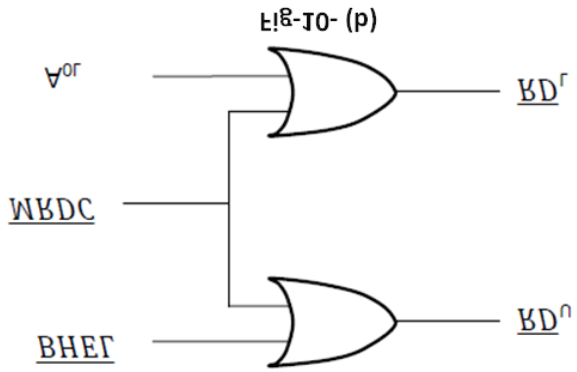


Fig-10- (b)

Data Bus Transceivers

The data bus transceiver block of the bus interface circuit can be implemented with 74F245 octal bus transceiver ICs. Figure-11- shows a block diagram of this device.

Note that its bidirectional input/output lines are called A1 throng A8 and B1 through B8. the $\overline{G}$ input is used to enable the buffer for operation. On the other hand, the logic level at the direction (DIR) input selects the direction in which data are transferred through the device.

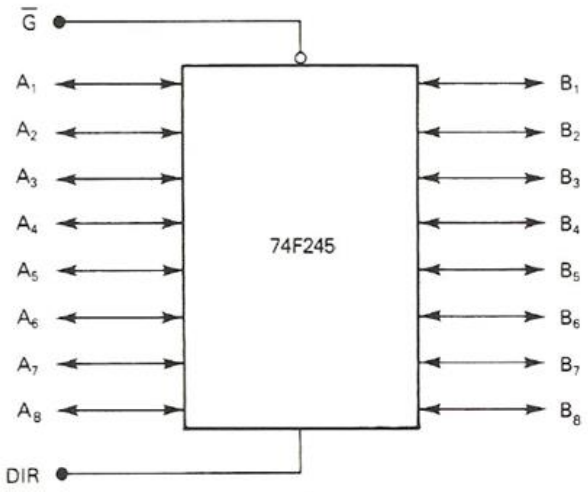


Fig-11-

Figure -12- shows a circuit that implements the data bus transceiver block of the bus interface circuit using the 74F245. For the 16-bit data bus of the 8086 microcomputer, two devices are required. Here the DIR input is driven by the signal data transmit/receive $DT/\overline{R}$, and $\bar{G}$ is supplied by data bus enable (DEN). These signals are outputs of the 8288 bus controller.

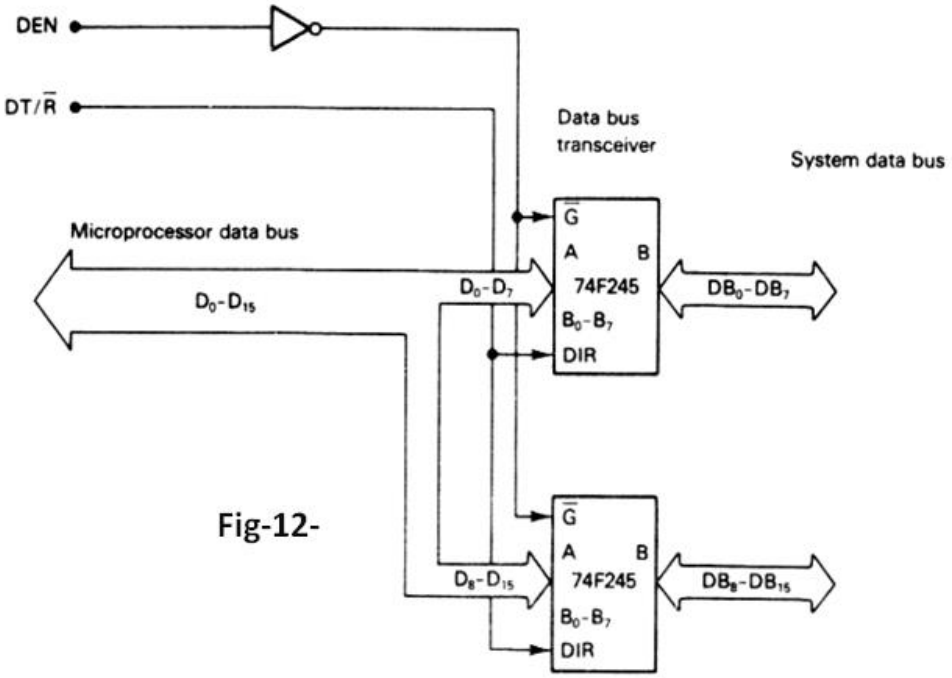


Fig-12-

Address Decoder

The circuit in Fig.-13- uses the 74F138 decoder (3-to- 8) to generate chip enable signals $\overline{CE_0}$ through $\overline{CE_7}$ by decoding address lines A_{17L}, A_{18L}, and A_{19L}. The G1 inputs must be tied to +5V permanently, while G2A and G2B input must be tied to ground permanently

.

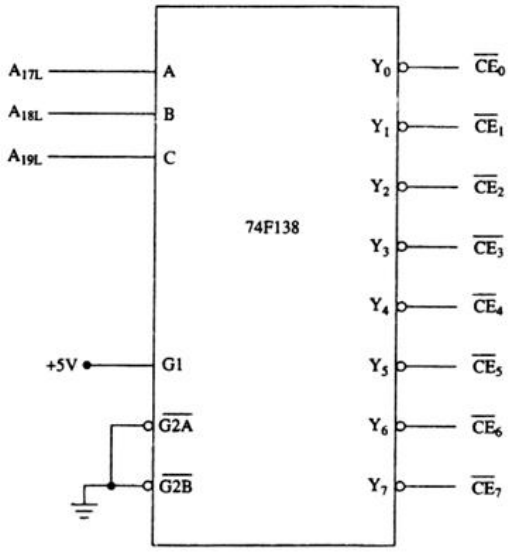


Fig-13-