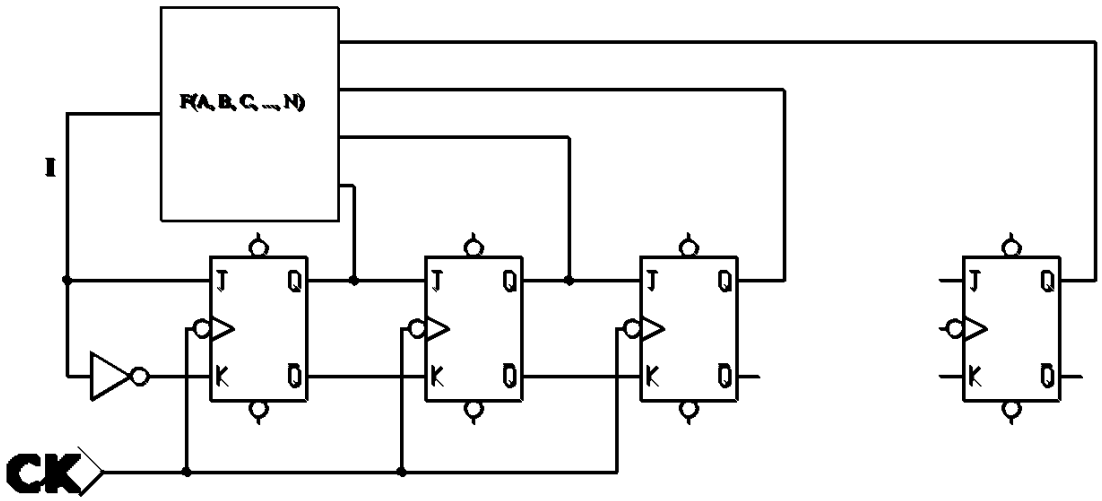
Sequence Generator

The fundamental structure of a sequence generator is shown in the figure below:



The sequence generator is a shift register of FIFO (first input first output) with input (I), where (I) is a combinational logic function of the outputs (N) produced from the flip-flops of the shift register. The sequence generator generates a sequence of binary bits (information). Thus, the length of the sequence is related to the number of flip-flops that are required to produce a sequence generator. The general equation is:

$$S \leq 2^n - 1$$

Where:

S = the length of the repeated sequence.

M = number of the sequence generator's flip-flops

Note:

If S = $2^n - 1$, then we have a maximum length of sequence generator.

Example: Design a sequence generator that generates the sequence "100010011010111"

Solution:

Since there is no repeated in the sequence, then;

$$S = 15\ bit$$

$$Since\ S \leq 2^n - 1$$

$$then\ 15 \leq 2^n - 1$$

$$2^n \geq 16$$

So, (**n)** is at least = 4, (i.e. four flip-flops are required to design the sequence generator; A, B, C & D).

Now we write a table to specify the operation of the sequence generator, also to design the logic circuit that generates the output (I).

Note, if a row in the table is repeated, then we must add another flip-flop to the sequence generator to remove the repetition case from the table.

D	C	B	A	I = f(A, B, C, D)
1	1	1	1	0
1	1	1	0	0
1	1	0	0	0
1	0	0	0	1
0	0	0	1	0
0	0	1	0	0
0	1	0	0	1
1	0	0	1	1
0	0	1	1	0
0	1	1	0	1
1	1	0	1	0
1	0	1	0	1
0	1	0	1	1
1	0	1	1	1
0	1	1	1	1
1	1	1	1	0
1	1	1	0	0
1	1	0	0	0

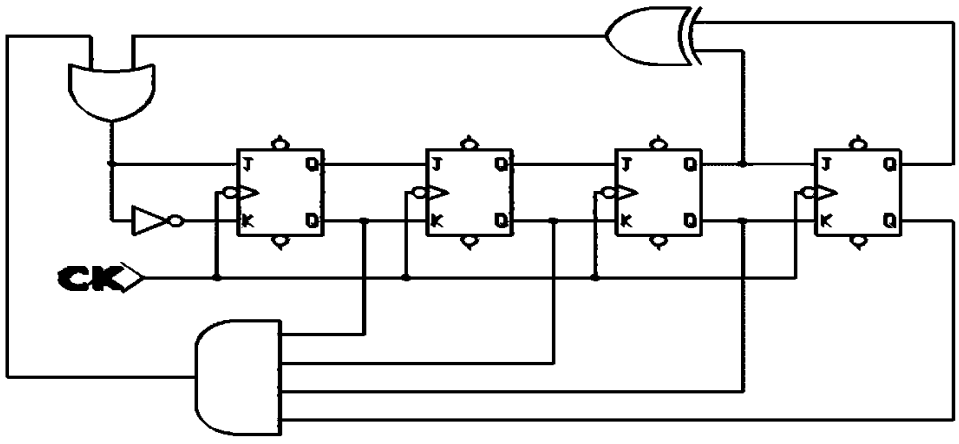
Repeated

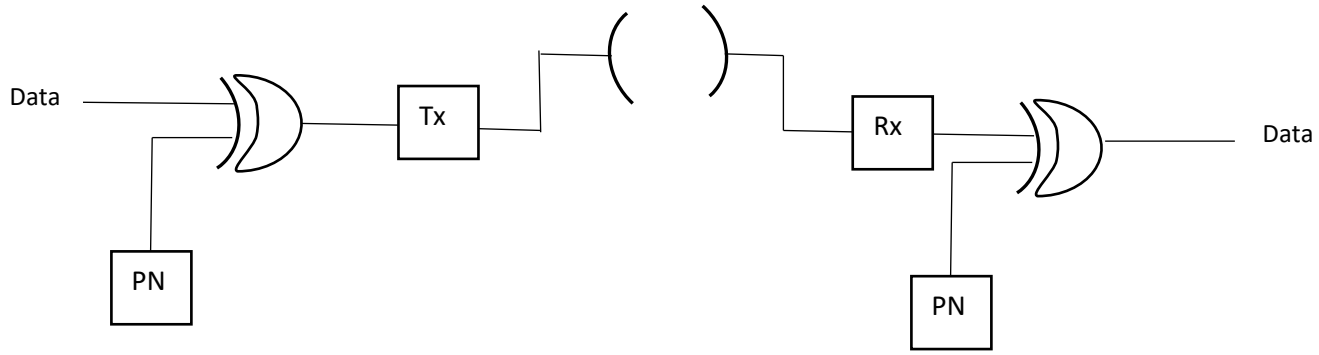
DC \ BA	00	01	11	10
00	X	0	0	0
01	1	1	1	1
11	0	0	0	0
10	1	1	1	1

$$I = \bar{C}D + C\bar{D}$$

$$= C \oplus D$$

The sequence generator logic circuit must be protected from the reset state (0000) by adding two logic gates to the circuit, are connected as follows: the AND-gate is anding $\bar{A}, \bar{B}, \bar{C}$ & $\bar{D}$, while the OR-gate is oring I and the output of AND-gate as shown in the figure below.





Note:

The sequence generator is also called pseudo noise (PN) generator.

H.W., discuss how we can use the PN generator in the transmitter (Tx) and receiver (Rx) circuits with a simple example?